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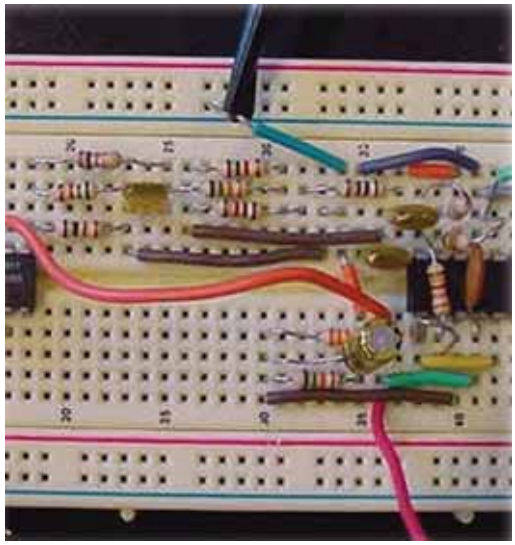
9

Transistor Biasing



INTRODUCTION

The basic function of transistor is to do amplification. The weak signal is given to the base of the transistor and amplified output is obtained in the collector circuit. One important requirement during amplification is that only the magnitude of the signal should increase and there should be no change in signal shape. This increase in magnitude of the signal without any change in shape is known as *faithful amplification*. In order to achieve this, means are provided to ensure that input circuit (*i.e.* base-emitter junction) of the transistor remains forward biased and output circuit (*i.e.* collector-base junction) always remains reverse biased during all parts of the signal. This is known as transistor biasing. In this chapter, we shall discuss how transistor biasing helps in achieving faithful amplification.

9.1 Faithful Amplification

The process of raising the strength of a weak signal without any change in its general shape is known as **faithful amplification.**

The theory of transistor reveals that it will function properly if its input circuit (*i.e.* base-emitter junction) remains forward biased and output circuit (*i.e.* collector-base junction) remains reverse biased at all times. This is then the key factor for achieving faithful amplification. To ensure this, the following basic conditions must be satisfied :

(*i*) Proper zero signal collector current

(*ii*) Minimum proper base-emitter voltage (V_{BE}) at any instant

(*iii*) Minimum proper collector-emitter voltage (V_{CE}) at any instant

The conditions (*i*) and (*ii*) ensure that base-emitter junction shall remain properly forward biased during all parts of the signal. On the other hand, condition (*iii*) ensures that base-collector junction shall remain properly reverse biased at all times. In other words, the fulfilment of these conditions will ensure that transistor works over the active region of the output characteristics *i.e.* between saturation to cut off.

(*i*) Proper zero signal collector current. Consider an *npn* transistor circuit shown in Fig. 9.1 (*i*). During the positive half-cycle of the signal, base is positive w.r.t. emitter and hence base-emitter junction is forward biased. This will cause a base current and much larger collector current to flow in the circuit. The result is that positive half-cycle of the signal is amplified in the collector as shown. However, during the negative half-cycle of the signal, base-emitter junction is reverse biased and hence no current flows in the circuit. The result is that there is no output due to the negative half-cycle of the signal. Thus we shall get an amplified output of the signal with its negative half-cycles completely cut off which is unfaithful amplification.

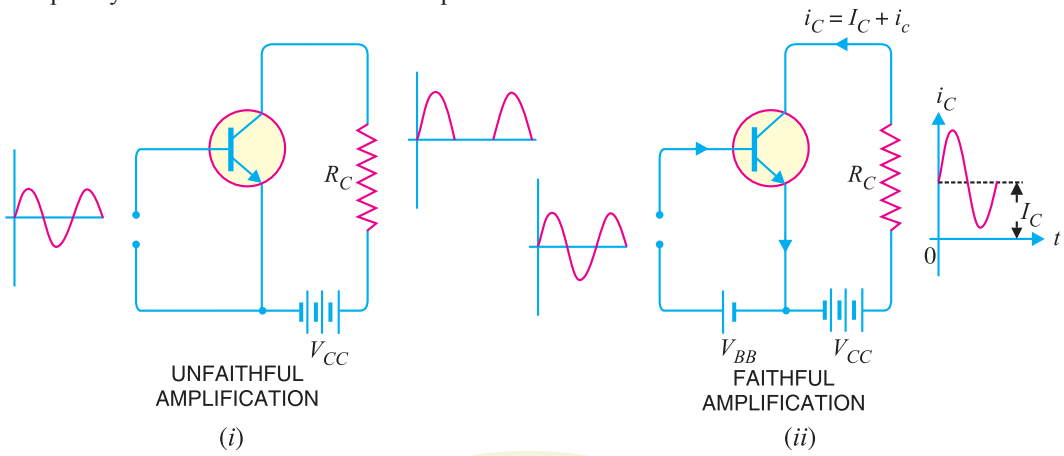


Fig. 9.1

Now, introduce a battery source V_{BB} in the base circuit as shown in Fig. 9.1 (*ii*). The magnitude of this voltage should be such that it keeps the input circuit forward biased even during the peak of negative half-cycle of the signal. When no signal is applied, a d.c. current I_C will flow in the collector circuit due to V_{BB} as shown. This is known as *zero signal collector current* I_C. During the positive half-cycle of the signal, input circuit is more forward biased and hence collector current increases. However, during the negative half-cycle of the signal, the input circuit is less forward biased and collector current decreases. In this way, negative half-cycle of the signal also appears in the output and hence faithful amplification results. It follows, therefore, that for faithful amplification, proper zero signal collector current must flow. *The value of zero signal collector current should be atleast equal to the maximum collector current due to signal alone i.e.*

Zero signal collector current ≥ Max. collector current due to signal alone

Illustration. Suppose a signal applied to the base of a transistor gives a peak collector current of 1mA. Then zero signal collector current must be atleast equal to 1mA so that even during the peak of negative half-cycle of the signal, there is no cut off as shown in Fig. 9.2 (*i*).

If zero signal collector current is less, say 0.5 mA as shown in Fig. 9.2 (*ii*), then some part (shaded portion) of the negative half-cycle of signal will be cut off in the output.

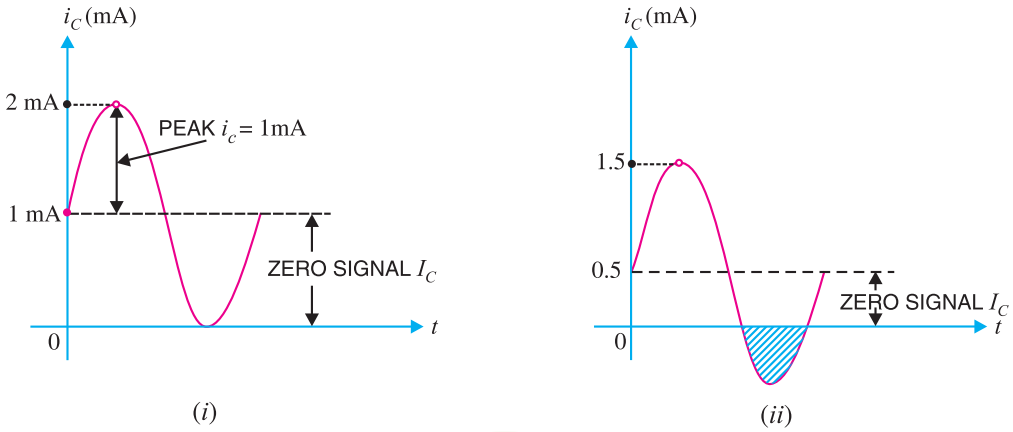


Fig. 9.2

(*ii*) Proper minimum base-emitter voltage. In order to achieve faithful amplification, the base-emitter voltage (V_{BE}) should not fall below 0.5V for germanium transistors and 0.7V for *Si* transistors at any instant.

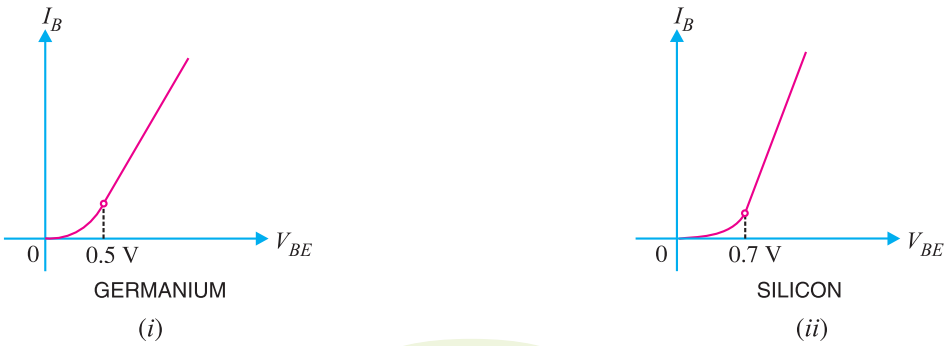


Fig. 9.3

The base current is very small until the *input voltage overcomes the potential barrier at the base-emitter junction. The value of this potential barrier is 0.5V for Ge transistors and 0.7V for *Si* transistors as shown in Fig. 9.3. Once the potential barrier is overcome, the base current and hence collector current increases sharply. Therefore, if base-emitter voltage V_{BE} falls below these values during any part of the signal, that part will be amplified to lesser extent due to small collector current. This will result in unfaithful amplification.

(*iii*) Proper minimum V_{CE} at any instant. For faithful amplification, the collector-emitter voltage V_{CE} should not fall below 0.5V for Ge transistors and 1V for silicon transistors. This is called *knee voltage* (See Fig. 9.4).

* In practice, a.c. signals have small voltage level (< 0.1V) and if applied directly will not give any collector current.

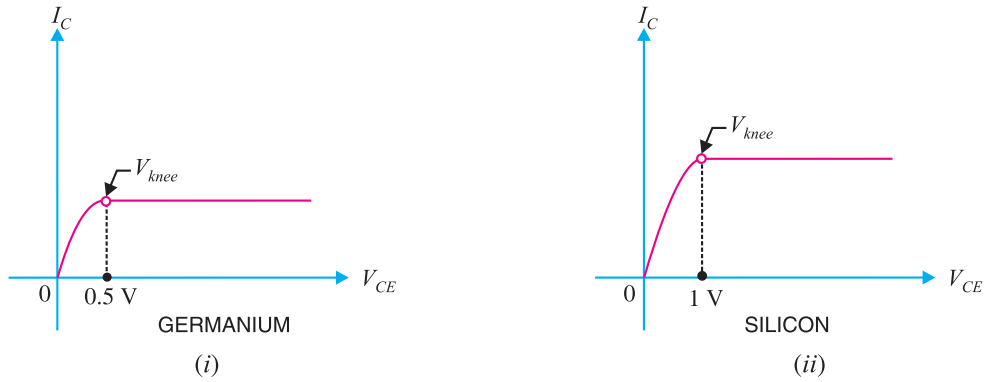


Fig. 9.4

When V_{CE} is too low (less than 0.5V for *Ge* transistors and 1V for *Si* transistors), the collector-base junction is not properly reverse biased. Therefore, the collector cannot attract the charge carriers emitted by the emitter and hence a greater portion of them goes to the base. This decreases the collector current while base current increases. Hence, value of β falls. Therefore, if V_{CE} is allowed to fall below V_{knee} during any part of the signal, that part will be less amplified due to reduced β. This will result in unfaithful amplification. However, when V_{CE} is greater than V_{knee}, the collector-base junction is properly reverse biased and the value of β remains constant, resulting in faithful amplification.

9.2 Transistor Biasing

It has already been discussed that for faithful amplification, a transistor amplifier must satisfy three basic conditions, namely : (*i*) proper zero signal collector current, (*ii*) proper base-emitter voltage at any instant and (*iii*) proper collector-emitter voltage at any instant. It is the fulfilment of these conditions which is known as transistor biasing.

The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as **transistor biasing.**

The basic purpose of transistor biasing is to keep the base-emitter junction properly forward biased and collector-base junction properly reverse biased during the application of signal. This can be achieved with a bias battery or associating a circuit with a transistor. The latter method is more efficient and is frequently employed. The circuit which provides transistor biasing is known as *biasing circuit*. It may be noted that transistor biasing is very essential for the proper operation of transistor in any circuit.

Example 9.1. *An npn silicon transistor has V_{CC} = 6 V and the collector load R_C = 2.5 kΩ. Find :*

(i) The maximum collector current that can be allowed during the application of signal for faithful amplification.

(ii) The minimum zero signal collector current required.

Solution. Collector supply voltage, V_{CC} = 6 V

Collector load, R_C = 2.5 kΩ

(*i*) We know that for faithful amplification, V_{CE} should not be less than 1V for silicon transistor.

$\therefore$ Max. voltage allowed across R_C = 6 – 1 = 5 V

$\therefore$ Max. allowed collector current = 5 V/R_C = 5 V/2.5 kΩ = **2 mA**

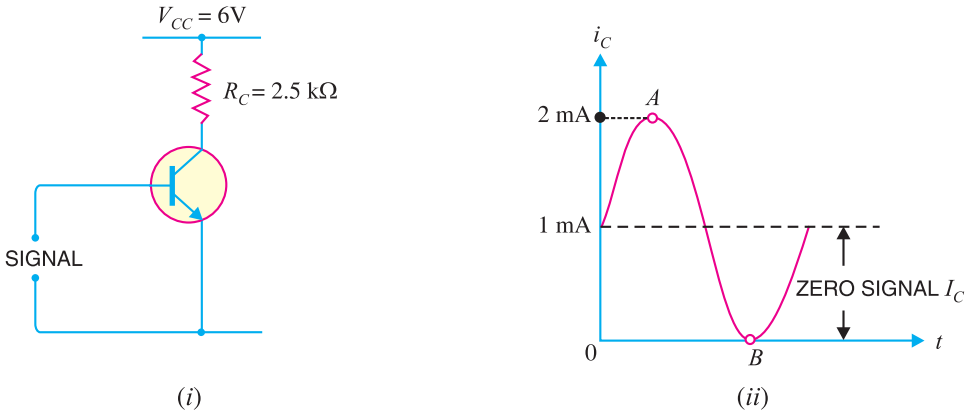


Fig. 9.5

Thus, the maximum collector current allowed during any part of the signal is 2 mA. If the collector current is allowed to rise above this value, V_{CE} will fall below 1 V. Consequently, value of β will fall, resulting in unfaithful amplification.

(ii) During the negative peak of the signal, collector current can at the most be allowed to become zero. As the negative and positive half cycles of the signal are equal, therefore, the change in collector current due to these will also be equal but in opposite direction.

∴ Minimum zero signal collector current required = 2 mA/2 = **1 mA**

During the positive peak of the signal [point *A* in Fig. 9.5 (*ii*)], $i_C = 1 + 1 = 2$mA and during the negative peak (point *B*),

$$i_C = 1 - 1 = 0 \text{ mA}$$

Example 9.2. *A transistor employs a 4 kΩ load and V_{CC} = 13V. What is the maximum input signal if β = 100 ? Given V_{knee} = 1V and a change of 1V in V_{BE} causes a change of 5mA in collector current.*

Solution.

Collector supply voltage, $V_{CC} = 13$ V

Knee voltage, $V_{knee} = 1$ V

Collector load, $R_C = 4$ kΩ

∴ Max. allowed voltage across $R_C = 13 - 1 = 12$ V

∴ Max. allowed collector current, $i_C = \dfrac{12 \text{ V}}{R_C} = \dfrac{12 \text{ V}}{4 \text{ k}\Omega} = 3$ mA

Maximum base current, $i_B = \dfrac{i_C}{\beta} = \dfrac{3 \text{ mA}}{100} = 30$ μA

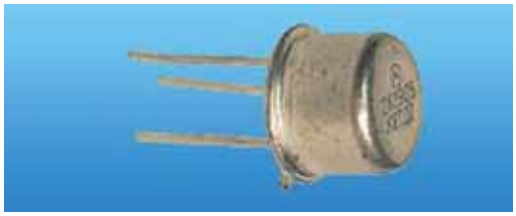
Now $\dfrac{\text{Collector current}}{\text{Base voltage (signal voltage)}} = 5$ mA/V

∴ Base voltage (signal voltage) $= \dfrac{\text{Collector current}}{5 \text{ mA/V}} = \dfrac{3 \text{ mA}}{5 \text{ mA/V}} =$ **600 mV**

9.3 Inherent Variations of Transistor Parameters

In practice, the transistor parameters such as β, V_{BE} are not the same for every transistor even of the same type. To give an example, BC147 is a silicon *npn* transistor with β varying from 100 to 600 *i.e.* β for one transistor may be 100 and for the other it may be 600, although both of them are *BC*147.

This large variation in parameters is a characteristic of transistors. The major reason for these variations is that transistor is a new device and manufacturing techniques have not too much advanced. For instance, it has not been possible to control the base width and it may vary, although slightly, from one transistor to the other even of the same type. Such small variations result in large change in transistor parameters such as β, V_{BE} etc.



Transistor

The inherent variations of transistor parameters may change the operating point, resulting in unfaithful amplification. It is, therefore, very important that biasing network be so designed that it should be able to work with all transistors of one type whatever may be the spread in β or V_{BE}. In other words, the operating point should be independent of transistor parameters variations.

9.4 Stabilisation

The collector current in a transistor changes rapidly when

(*i*) the temperature changes,

(*ii*) the transistor is replaced by another of the same type. This is due to the inherent variations of transistor parameters.

When the temperature changes or the transistor is replaced, the operating point (*i.e.* zero signal I_C and V_{CE}) also changes. However, for faithful amplification, it is essential that operating point remains fixed. This necessitates to make the operating point independent of these variations. This is known as stabilisation.

The process of making operating point independent of temperature changes or variations in transistor parameters is known as **stabilisation.**

Once stabilisation is done, the zero signal I_C and V_{CE} become independent of temperature variations or replacement of transistor *i.e.* the operating point is fixed. A good biasing circuit always ensures the stabilisation of operating point.

Need for stabilisation. Stabilisation of the operating point is necessary due to the following reasons :

(*i*) Temperature dependence of I_C

(*ii*) Individual variations

(*iii*) Thermal runaway

(*i*) Temperature dependence of I_C. The collector current I_C for CE circuit is given by:

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO}$$

The collector leakage current I_{CBO} is greatly influenced (especially in germanium transistor) by temperature changes. A rise of 10°C doubles the collector leakage current which may be as high as 0.2 mA for low powered germanium transistors. As biasing conditions in such transistors are generally so set that zero signal I_C = 1mA, therefore, the change in I_C due to temperature variations cannot be tolerated. This necessitates to stabilise the operating point *i.e.* to hold I_C constant inspite of temperature variations.

(*ii*) Individual variations. The value of β and V_{BE} are not exactly the same for any two transistors even of the same type. Further, V_{BE} itself decreases when temperature increases. When a transistor is replaced by another of the same type, these variations change the operating point. This necessitates to stabilise the operating point *i.e.* to hold I_C constant irrespective of individual variations in transistor parameters.

(*iii*) Thermal runaway. The collector current for a *CE* configuration is given by :

$$I_C = \beta I_B + (\beta + 1) I_{CBO} \qquad ...(i)$$

The collector leakage current I_{CBO} is strongly dependent on temperature. The flow of collector current produces heat within the transistor. This raises the transistor temperature and if no stabilisation is done, the collector leakage current I_{CBO} also increases. It is clear from exp. (*i*) that if I_{CBO} increases, the collector current I_C increases by $(\beta + 1)\, I_{CBO}$. The increased I_C will raise the temperature of the transistor, which in turn will cause I_{CBO} to increase. This effect is cumulative and in a matter of seconds, the collector current may become very large, causing the transistor to burn out.

The self-destruction of an unstabilised transistor is known as **thermal runaway.**

In order to avoid thermal runaway and consequent destruction of transistor, it is very essential that operating point is stabilised *i.e.* I_C is kept constant. In practice, this is done by causing I_B to decrease automatically with temperature increase by circuit modification. Then decrease in βI_B will compensate for the increase in $(\beta + 1)\, I_{CBO}$, keeping I_C nearly constant. In fact, this is what is always aimed at while building and designing a biasing circuit.

9.5 Essentials of a Transistor Biasing Circuit

It has already been discussed that transistor biasing is required for faithful amplification. The biasing network associated with the transistor should meet the following requirements :

(*i*) It should ensure proper zero signal collector current.

(*ii*) It should ensure that V_{CE} does not fall below 0.5 V for *Ge* transistors and 1 V for silicon transistors at any instant.

(*iii*) It should ensure the stabilisation of operating point.

9.6 Stability Factor

It is desirable and necessary to keep I_C constant in the face of variations of I_{CBO} (sometimes represented as I_{CO}). The extent to which a biasing circuit is successful in achieving this goal is measured by stability factor *S*. It is defined as under :

The rate of change of collector current I_C w.r.t. the collector leakage current *I_{CO} *at constant β and I_B is called* **stability factor** *i.e.*

$$\text{Stability factor, } S = \frac{dI_C}{dI_{CO}} \text{ at constant } I_B \text{ and } \beta$$

The stability factor indicates the change in collector current I_C due to the change in collector leakage current I_{CO}. Thus a stability factor 50 of a circuit means that I_C changes 50 times as much as any change in I_{CO}. In order to achieve greater thermal stability, it is desirable to have as low stability factor as possible. The ideal value of *S* is 1 but it is never possible to achieve it in practice. Experience shows that values of S exceeding 25 result in unsatisfactory performance.

The general expression of stability factor for a C.E. configuration can be obtained as under:

$$I_C = \beta I_B + (\beta + 1)\, I_{CO}$$

** Differentiating above expression *w.r.t.* I_C, we get,

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

or
$$1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S} \qquad \left[\because \frac{dI_{CO}}{dI_C} = \frac{1}{S}\right]$$

or
$$S = \frac{\beta + 1}{1 - \beta\left(\dfrac{dI_B}{dI_C}\right)}$$

* $I_{CBO} = I_{CO}$ = collector leakage current in *CB* arrangement

** Assuming β to be independent of I_C.

9.7 Methods of Transistor Biasing

In the transistor amplifier circuits drawn so far biasing was done with the aid of a battery V_{BB} which was separate from the battery V_{CC} used in the output circuit. However, in the interest of simplicity and economy, it is desirable that transistor circuit should have a single source of supply—the one in the output circuit (*i.e.* V_{CC}). The following are the most commonly used methods of obtaining transistor biasing from one source of supply (*i.e.* V_{CC}) :

(*i*) Base resistor method

(*ii*) Emitter bias method

(*iii*) Biasing with collector-feedback resistor

(*iv*) Voltage-divider bias

In all these methods, the same basic principle is employed *i.e.* required value of base current (and hence I_C) is obtained from V_{CC} in the zero signal conditions. The value of collector load R_C is selected keeping in view that V_{CE} should not fall below 0.5 V for germanium transistors and 1 V for silicon transistors.

For example, if $\beta = 100$ and the zero signal collector current I_C is to be set at 1mA, then I_B is made equal to $I_C/\beta = 1/100 = 10\ \mu A$. Thus, the biasing network should be so designed that a base current of 10 μA flows in the zero signal conditions.

9.8 Base Resistor Method

In this method, a high resistance R_B (several hundred kΩ) is connected between the base and +ve end of supply for *npn* transistor (See Fig. 9.6) and between base and negative end of supply for *pnp* transistor. Here, the required zero signal base current is provided by V_{CC} and it flows through R_B. It is because now base is positive *w.r.t.* emitter *i.e.* base-emitter junction is forward biased. The required value of zero signal base current I_B (and hence $I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor R_B.

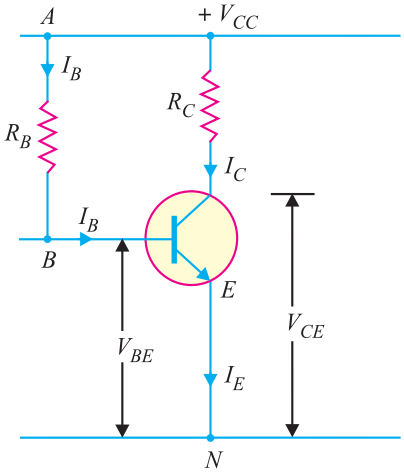


Fig. 9.6

Circuit analysis. It is required to find the value of R_B so that required collector current flows in the zero signal conditions. Let I_C be the required zero signal collector current.

$$\therefore \qquad I_B = \frac{I_C}{\beta}$$

Considering the closed circuit *ABENA* and applying Kirchhoff's voltage law, we get,

$$V_{CC} = I_B R_B + V_{BE}$$

or $$I_B R_B = V_{CC} - V_{BE}$$

$$\therefore \qquad R_B = \frac{V_{CC} - V_{BE}}{I_B} \qquad \ldots (i)$$

As V_{CC} and I_B are known and V_{BE} can be seen from the transistor manual, therefore, value of R_B can be readily found from exp. (*i*).

Since V_{BE} is generally quite small as compared to V_{CC}, the former can be neglected with little error. It then follows from exp. (*i*) that :

$$R_B = \frac{V_{CC}}{I_B}$$

It may be noted that V_{CC} is a fixed known quantity and I_B is chosen at some suitable value. Hence, R_B can always be found directly, and for this reason, this method is sometimes called *fixed-bias method*.

Stability factor. As shown in Art. 9.6,

$$\text{Stability factor,} \quad S = \frac{\beta + 1}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

In fixed-bias method of biasing, I_B is independent of I_C so that $dI_B/dI_C = 0$. Putting the value of $dI_B / dI_C = 0$ in the above expression, we have,

$$\text{Stability factor,} \quad S = \beta + 1$$

Thus the stability factor in a fixed bias is $(\beta + 1)$. This means that I_C changes $(\beta + 1)$ times as much as any change in I_{CO}. For instance, if $\beta = 100$, then $S = 101$ which means that I_C increases 101 times faster than I_{CO}. Due to the large value of S in a fixed bias, it has poor thermal stability.

Advantages :

(*i*) This biasing circuit is very simple as only one resistance R_B is required.

(*ii*) Biasing conditions can easily be set and the calculations are simple.

(*iii*) There is no loading of the source by the biasing circuit since no resistor is employed across base-emitter junction.

Disadvantages :

(*i*) This method provides poor stabilisation. It is because there is no means to stop a self-increase in collector current due to temperature rise and individual variations. For example, if β increases due to transistor replacement, then I_C also increases by the same factor as I_B is constant.

(*ii*) The stability factor is very high. Therefore, there are strong chances of thermal runaway.

Due to these disadvantages, this method of biasing is rarely employed.

Example 9.3. *Fig. 9.7 (i) shows biasing with base resistor method. (i) Determine the collector current I_C and collector-emitter voltage V_{CE}. Neglect small base-emitter voltage. Given that $\beta = 50$.*

(ii) If R_B in this circuit is changed to 50 kΩ, find the new operating point.

Solution.

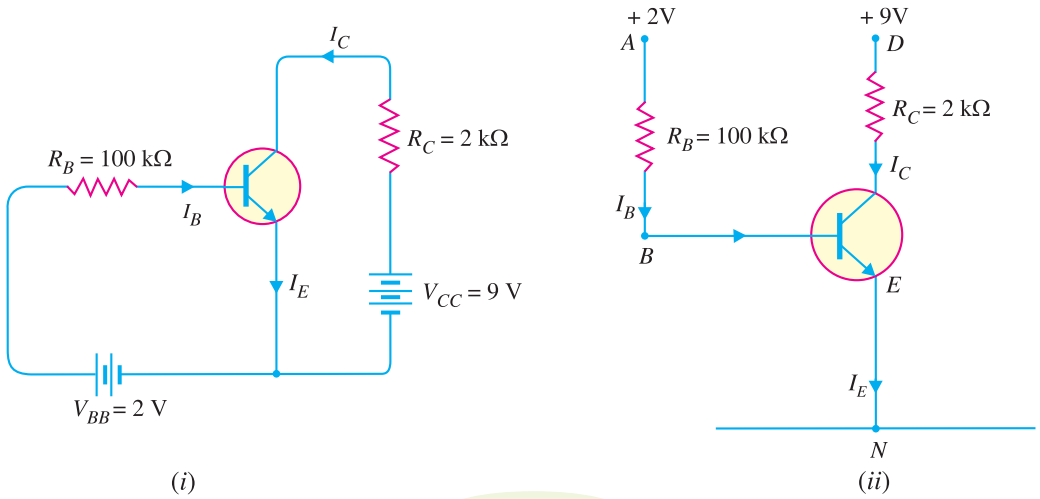


Fig. 9.7

In the circuit shown in Fig. 9.7 (*i*), biasing is provided by a battery V_{BB} (= 2V) in the base circuit which is separate from the battery V_{CC} (= 9V) used in the output circuit. The same circuit is shown in a simplified way in Fig. 9.7 (*ii*). Here, we need show only the supply voltages, + 2V and + 9V. It may be noted that negative terminals of the power supplies are grounded to get a complete path of current.

(*i*) Referring to Fig.9.7 (*ii*) and applying Kirchhoff 's voltage law to the circuit *ABEN*, we get,

$$I_B R_B + V_{BE} = 2\text{ V}$$

As V_{BE} is negligible,

$$\therefore \quad I_B = \frac{2\text{V}}{R_B} = \frac{2\text{V}}{100\text{ k}\Omega} = 20\ \mu\text{A}$$

$$\text{Collector current, } I_C = \beta I_B = 50 \times 20\ \mu\text{A} = 1000\ \mu\text{A} = \mathbf{1\ mA}$$

Applying Kirchhoff's voltage law to the circuit *DEN*, we get,

$$I_C R_C + V_{CE} = 9$$

or $$1\text{ mA} \times 2\text{ k}\Omega + V_{CE} = 9$$

or $$V_{CE} = 9 - 2 = \mathbf{7\ V}$$

(*ii*) When R_B is made equal to 50 kΩ, then it is easy to see that base current is doubled *i.e.* $I_B = 40\ \mu\text{A}$.

$$\therefore \quad \text{Collector current, } I_C = \beta I_B = 50 \times 40 = 2000\ \mu\text{A} = 2\text{ mA}$$

$$\text{Collector-emitter voltage, } V_{CE} = V_{CC} - I_C R_C = 9 - 2\text{ mA} \times 2\text{ k}\Omega = 5\text{ V}$$

∴ New operating point is **5 V, 2 mA.**

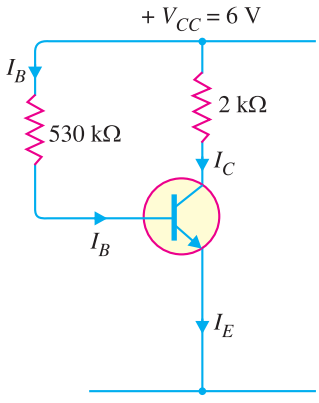
Example 9.4. *Fig. 9.8 (i) shows that a silicon transistor with β = 100 is biased by base resistor method. Draw the d.c. load line and determine the operating point. What is the stability factor ?*

Solution. $V_{CC} = 6\text{ V}, R_B = 530\text{ k}\Omega, R_C = 2\text{ k}\Omega$

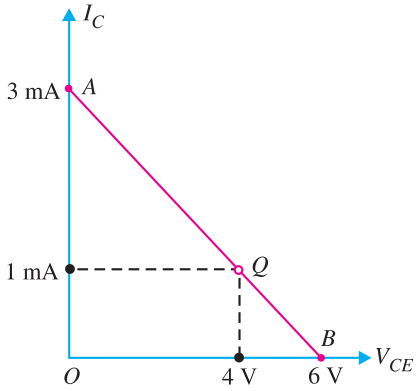
D.C. load line. Referring to Fig. 9.8 (*i*), $V_{CE} = V_{CC} - I_C R_C$

When $I_C = 0$, $V_{CE} = V_{CC} = 6$ V. This locates the first point *B* (*OB* = 6V) of the load line on collector-emitter voltage axis as shown in Fig. 9.8 (*ii*).

When $V_{CE} = 0$, $I_C = V_{CC}/R_C = 6\text{V}/2\text{ k}\Omega = 3$ mA. This locates the second point *A* (*OA* = 3mA) of the load line on the collector current axis. By joining points *A* and *B*, d.c. load line *AB* is constructed [See Fig. 9.8 (*ii*)].



(*i*)



(*ii*)

Fig. 9.8

Operating point Q. As it is a silicon transistor, therefore, $V_{BE} = 0.7V$. Referring to Fig. 9.8 (*i*), it is clear that :

$$I_B R_B + V_{BE} = V_{CC}$$

or $$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{(6 - 0.7)\ V}{530\ k\Omega} = 10\ \mu A$$

$\therefore$ Collector current, $I_C = \beta I_B = 100 \times 10 = 1000\ \mu A = 1\ mA$

Collector-emitter voltage, $V_{CE} = V_{CC} - I_C R_C = 6 - 1\ mA \times 2\ k\Omega = 6 - 2 = 4\ V$

$\therefore$ Operating point is **4 V, 1 mA.**

Fig. 9.8 (*ii*) shows the operating point Q on the d.c. load line. Its co-ordinates are $I_C = 1mA$ and $V_{CE} = 4V$.

Stability factor $= \beta + 1 = 100 + 1 =$ **101**

Example 9.5. *(i) A germanium transistor is to be operated at zero signal $I_C = 1mA$. If the collector supply $V_{CC} = 12V$, what is the value of R_B in the base resistor method ? Take $\beta = 100$.*

(ii) If another transistor of the same batch with $\beta = 50$ is used, what will be the new value of zero signal I_C for the same R_B ?

Solution. $V_{CC} = 12\ V, \quad \beta = 100$

As it is a *Ge* transistor, therefore,

$V_{BE} = 0.3\ V$

(*i*) Zero signal $I_C = 1\ mA$

$\therefore$ Zero signal $I_B = I_C/\beta = 1\ mA/100 = 0.01\ mA$

Using the relation, $V_{CC} = I_B R_B + V_{BE}$

$\therefore$ $$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12 - 0.3}{0.01\ mA}$$

$$= 11.7\ V/0.01\ mA = \textbf{1170 k}\Omega$$

(*ii*) Now $\beta = 50$

Again using the relation, $V_{CC} = I_B R_B + V_{BE}$

$\therefore$ $$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.3}{1170\ k\Omega}$$

$$= 11.7\ V/1170\ k\Omega = 0.01\ mA$$

$\therefore$ Zero signal $I_C = \beta I_B = 50 \times 0.01 =$ **0.5 mA**

Comments. It is clear from the above example that with the change in transistor parameter β, the zero signal collector current has changed from 1mA to 0.5mA. Therefore, base resistor method cannot provide stabilisation.

Example 9.6. *Calculate the values of three currents in the circuit shown in Fig. 9.9.*

Solution. Applying Kirchhoff's voltage law to the base side and taking resistances in kΩ and currents in mA, we have,

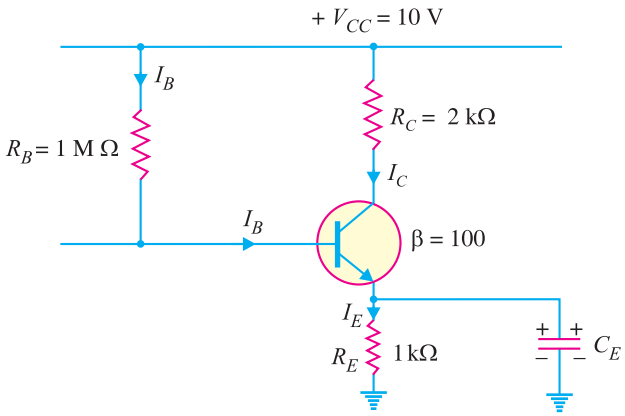


Fig. 9.9

$$V_{CC} = I_B R_B + V_{BE} + I_E \times 1$$

or $$10 = 1000\, I_B + *0 + (I_C + I_B)$$

or $$10 = 1000\, I_B + (\beta\, I_B + I_B)$$

or $$10 = 1000\, I_B + (100\, I_B + I_B)$$

or $$10 = 1101\, I_B$$

$\therefore$ $$I_B = 10/1101 = \mathbf{0.0091\ mA}$$

$$I_C = \beta\, I_B = 100 \times 0.0091 = \mathbf{0.91\ mA}$$

$$I_E = I_C + I_B = 0.91 + 0.0091 = \mathbf{0.919\ mA}$$

Example 9.7. *Design base resistor bias circuit for a CE amplifier such that operating point is V_{CE} = 8V and I_C = 2 mA. You are supplied with a fixed 15V d.c. supply and a silicon transistor with β = 100. Take base-emitter voltage V_{BE} = 0.6V. Calculate also the value of load resistance that would be employed.*

Solution. Fig. 9.10 shows *CE* amplifier using base resistor method of biasing.

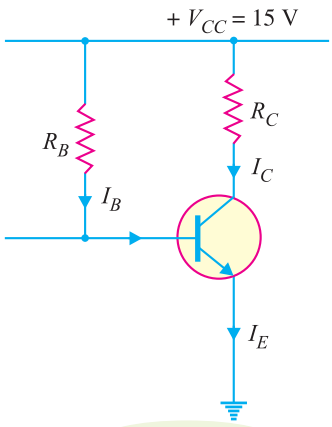


Fig. 9.10

$$V_{CC} = 15\ \text{V};\ \beta = 100;\ V_{BE} = 0.6\text{V}$$

$$V_{CE} = 8\ \text{V};\ I_C = 2\ \text{mA};\ R_C = ?;\ R_B = ?$$

$$V_{CC} = V_{CE} + I_C R_C$$

or $$15\ \text{V} = 8\ \text{V} + 2\ \text{mA} \times R_C$$

$\therefore$ $$R_C = \frac{(15 - 8)\ \text{V}}{2\text{mA}} = \mathbf{3.5\ k\Omega}$$

$$I_B = I_C/\beta = 2/100 = 0.02\ \text{mA}$$

$$V_{CC} = I_B R_B + V_{BE}$$

* Neglecting V_{BE} as it is generally very small.

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{(15 - 0.6)\ \text{V}}{0.02\ \text{mA}} = \mathbf{720\ k\Omega}$$

Example 9.8. *A *base bias circuit in Fig. 9.11 is subjected to an increase in temperature from 25°C to 75°C. If β = 100 at 25°C and 150 at 75°C, determine the percentage change in Q-point values (V_{CE} and I_C) over this temperature range. Neglect any change in V_{BE} and the effects of any leakage current.*

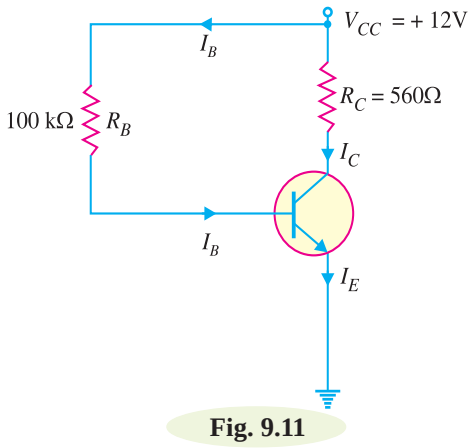


Fig. 9.11

Solution.

At 25°C

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\ V - 0.7\ V}{100\ k\Omega} = 0.113\ \text{mA}$$

$$\therefore \quad I_C = \beta I_B = 100 \times 0.113\ \text{mA} = 11.3\ \text{mA}$$

and $$V_{CE} = V_{CC} - I_C R_C = 12\text{V} - (11.3\ \text{mA})\ (560\Omega) = 5.67\text{V}$$

At 75 °C

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\ \text{V} - 0.7\ \text{V}}{100\ \text{k}\Omega} = 0.113\ \text{mA}$$

$$\therefore \quad I_C = \beta I_B = 150 \times 0.113\ \text{mA} = 17\ \text{mA}$$

and $$V_{CE} = V_{CC} - I_C R_C = 12\text{V} - (17\ \text{mA})\ (560\ \Omega) = 2.48\text{V}$$

$$\%\text{age change in } I_C = \frac{I_{C\,(75°C)} - I_{C\,(25°C)}}{I_{C\,(25°C)}} \times 100$$

$$= \frac{17\ \text{mA} - 11.3\ \text{mA}}{11.3\ \text{mA}} \times 100 = \mathbf{50\%}\ (\textit{increase})$$

Note that I_C changes by the same percentage as β.

$$\%\text{age change in } V_{CE} = \frac{V_{CE\,(75°C)} - V_{CE\,(25°C)}}{V_{CE\,(25°C)}} \times 100$$

$$= \frac{2.48\text{V} - 5.67\text{V}}{5.67\text{V}} \times 100 = \mathbf{-56.3\%}\ (\textit{decrease})$$

Comments. It is clear from the above example that Q-point is extremely dependent on β in a base bias circuit. Therefore, base bias circuit is very unstable. Consequently, this method is normally not used if linear operation is required. However, it can be used for switching operation.

Example 9.9. *In base bias method, how Q-point is affected by changes in V_{BE} and I_{CBO}.*

Solution. In addition to being affected by change in β, the Q-point is also affected by changes in V_{BE} and I_{CBO} in the base bias method.

***(i)* Effect of V_{BE}.** The base-emitter-voltage V_{BE} decreases with the increase in temperature (and vice-versa). The expression for I_B in base bias method is given by ;

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

* Note that base resistor method is also called *base bias method.*

It is clear that decrease in V_{BE} increases I_B. This will shift the Q-point ($I_C = \beta I_B$ and $V_{CE} = V_{CC} - I_C R_C$). The effect of change in V_{BE} is negligible if $V_{CC} >> V_{BE}$ (V_{CC} atleast 10 times greater than V_{BE}).

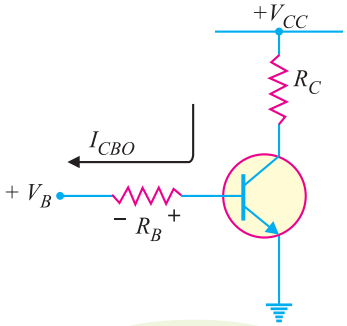


Fig. 9.12

(ii) Effect of I_{CBO}. The reverse leakage current I_{CBO} has the effect of decreasing the net base current and thus increasing the base voltage. It is because the flow of I_{CBO} creates a voltage drop across R_B that adds to the base voltage as shown in Fig. 9.12. Therefore, change in I_{CBO} shifts the Q-point of the base bias circuit. However, in modern transistors, I_{CBO} is usually less than 100 nA and its effect on the bias is negligible if $V_{BB} >> I_{CBO} R_B$.

Example 9.10. *Fig. 9.13 (i) shows the base resistor transistor circuit. The device (i.e. transistor) has the characteristics shown in Fig. 9.13 (ii). Determine V_{CC}, R_C and R_B.*

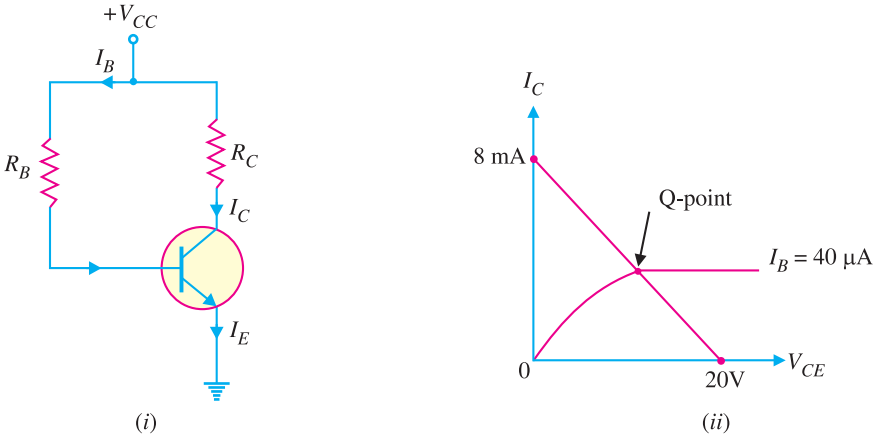


Fig. 9.13

Solution. From the d.c load line, $V_{CC} = 20V$.

$$\text{Max. } I_C = \frac{V_{CC}}{R_C} \text{ (when } V_{CE} = 0V)$$

$$\therefore \quad R_C = \frac{V_{CC}}{\text{Max. } I_C} = \frac{20V}{8mA} = 2.5\ k\Omega$$

$$\text{Now} \quad I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20V - 0.7V}{40\ \mu A} = \frac{19.3V}{40\ \mu A} = 482.5\ k\Omega$$

Example 9.11. *What fault is indicated in (i) Fig. 9.14 (i) and (ii) Fig. 9.14 (ii) ?*

Solution.

(i) The obvious fault in Fig. 9.14 (*i*) is that the **base is internally open.** It is because 3V at the base and 9V at the collector mean that transistor is in cut-off state.

(ii) The obvious fault in Fig. 9.14 (*ii*) is that **collector is internally open.** The voltage at the base is correct. The voltage of 9V appears at the collector because the 'open' prevents collector current.

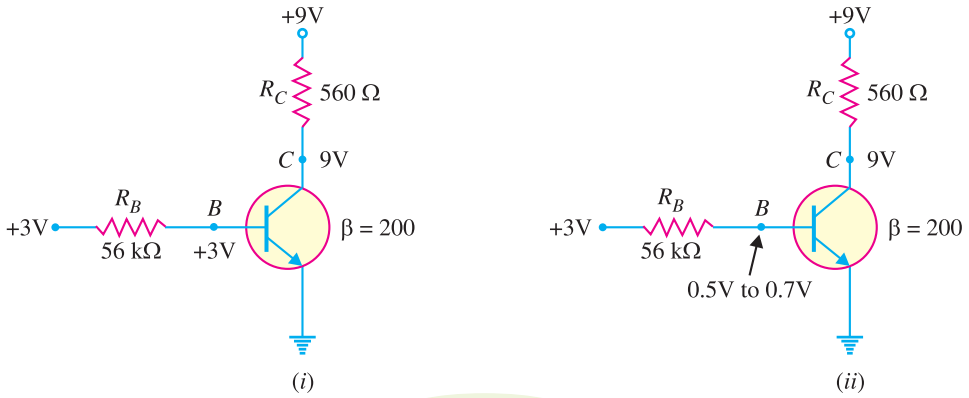


Fig. 9.14

9.9 Emitter Bias Circuit

Fig. 9.15 shows the emitter bias circuit. This circuit differs from base-bias circuit in two important respects. First, it uses two separate d.c. voltage sources ; one positive ($+V_{CC}$) and the other negative ($-V_{EE}$). Normally, the two supply voltages will be equal. For example, if $V_{CC} = +20$V (d.c.), then $V_{EE} = -20$V (d.c.). Secondly, there is a resistor R_E in the emitter circuit.

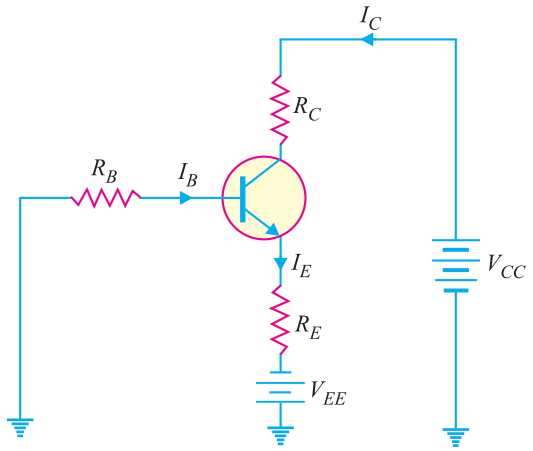


Fig. 9.15

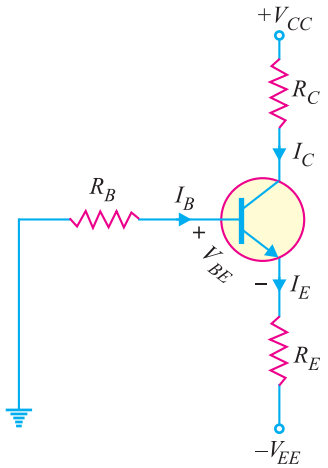


Fig. 9.16

We shall first redraw the circuit in Fig. 9.15 as it usually appears on schematic diagrams. This means deleting the battery symbols as shown in Fig. 9.16. All the information is still (See Fig. 9.16) on the diagram except that it is in condensed form. That is a negative supply voltage $-V_{EE}$ is applied to the bottom of R_E and a positive voltage of $+V_{CC}$ to the top of R_C.

9.10 Circuit Analysis of Emitter Bias

Fig. 9.16 shows the emitter bias circuit. We shall find the Q-point values (*i.e.* d.c. I_C and d.c. V_{CE}) for this circuit.

(*i*) Collector current (I_C). Applying Kirchhoff's voltage law to the base-emitter circuit in Fig. 9.16, we have,

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$\therefore \quad V_{EE} = I_B R_B + V_{BE} + I_E R_E$$

Now $I_C \simeq I_E$ and $I_C = \beta I_B \quad \therefore I_B \simeq \dfrac{I_E}{\beta}$

Putting $I_B = I_E/\beta$ in the above equation, we have,

$$V_{EE} = \left(\frac{I_E}{\beta}\right) R_B + I_E R_E + V_{BE}$$

or $$V_{EE} - V_{BE} = I_E (R_B/\beta + R_E)$$

$$\therefore \quad I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

Since $I_C \simeq I_E$, we have,

$$I_C = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

(*ii*) Collector-emitter voltage (V_{CE}). Fig. 9.17 shows the various voltages of the emitter bias circuit w.r.t. ground.

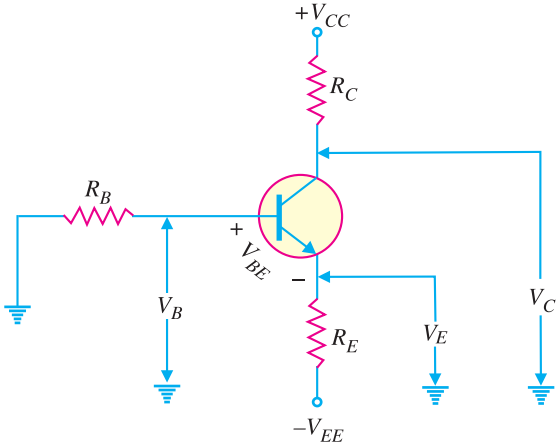


Fig. 9.17

Emitter voltage w.r.t. ground is

$$V_E = -V_{EE} + I_E R_E$$

Base voltage w.r.t. ground is

$$V_B = V_E + V_{BE}$$

Collector voltage w.r.t. ground is

$$V_C = V_{CC} - I_C R_C$$

Subtracting V_E from V_C and using the approximation $I_C \simeq I_E$, we have,

$$V_C - V_E = (V_{CC} - I_C R_C) - (-V_{EE} + I_C R_E) \qquad (\because I_E \simeq I_C)$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E)$$

Alternatively. Applying Kirchhoff's voltage law to the collector side of the emitter bias circuit in Fig. 9.16 (Refer back), we have,

$$V_{CC} - I_C R_C - V_{CE} - I_C^* R_E + V_{EE} = 0$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E)$$

Stability of Emitter bias. The expression for collector current I_C for the emitter bias circuit is given by ;

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

* $I_C \simeq I_E$

It is clear that I_C is dependent on V_{BE} and β, both of which change with temperature.

If $R_E >> R_B/\beta$, then expression for I_C becomes :

$$I_C = \frac{V_{EE} - V_{BE}}{R_E}$$

This condition makes $I_C (\simeq I_E)$ independent of β.

If $V_{EE} >> V_{BE}$, then I_C becomes :

$$I_C (\simeq I_E) = \frac{V_{EE}}{R_E}$$

This condition makes $I_C (\simeq I_E)$ independent of V_{BE}.

If $I_C (\simeq I_E)$ is independent of β and V_{BE}, the Q-point is not affected appreciably by the variations in these parameters. Thus emitter bias can provide stable Q-point if properly designed.

Example 9.12. *For the emitter bias circuit shown in Fig. 9.18, find I_E, I_C, V_C and V_{CE} for $\beta = 85$ and $V_{BE} = 0.7V$.*

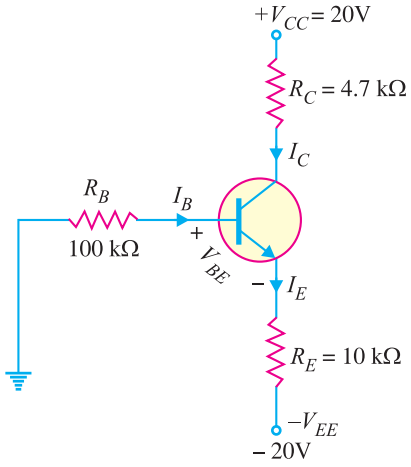


Fig. 9.18

Solution.

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{20V - 0.7V}{10\ k\Omega + 100\ k\Omega/85} = \mathbf{1.73\ mA}$$

$$V_C = V_{CC} - I_C R_C = 20V - (1.73\ mA)(4.7\ k\Omega) = \mathbf{11.9V}$$

$$V_E = -V_{EE} + I_E R_E = -20V + (1.73\ mA)(10\ k\Omega) = -2.7V$$

$$\therefore \quad V_{CE} = V_C - V_E = 11.9 - (-2.7V) = \mathbf{14.6V}$$

Note that operating point (or Q – point) of the circuit is 14.6V, 1.73 mA.

Example 9.13. *Determine how much the Q-point in Fig. 9.18 (above) will change over a temperature range where β increases from 85 to 100 and V_{BE} decreases from 0.7V to 0.6V.*

Solution.

For β = 85 and V_{BE} = 0.7V

As calculated in the above example, $I_C = 1.73$ mA and $V_{CE} = 14.6V$.

For β = 100 and V_{BE} = 0.6V

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{20V - 0.6V}{10\ k\Omega + 100\ k\Omega/100} = \frac{19.4V}{11\ k\Omega} = 1.76\ mA$$

$$V_C = V_{CC} - I_C R_C = 20V - (1.76\ mA)(4.7\ k\Omega) = 11.7V$$

$$V_E = -V_{EE} + I_E R_E = -20V + (1.76\ mA)(10\ k\Omega) = -2.4V$$

$$\therefore \quad V_{CE} = V_C - V_E = 11.7 - (-2.4) = 14.1\text{V}$$

$$\% \text{ age change in } I_C = \frac{1.76\text{ mA} - 1.73\text{ mA}}{1.73\text{ mA}} \times 100 = \mathbf{1.7\%}\ (\textit{increase})$$

$$\% \text{ age change in } V_{CE} = \frac{14.1\text{V} - 14.6\text{V}}{14.1\text{V}} \times 100 = \mathbf{-3.5\%}\ (\textit{decrease})$$

9.11 Biasing with Collector Feedback Resistor

In this method, one end of R_B is connected to the base and the other end to the collector as shown in Fig. 9.19. Here, the required zero signal base current is determined *not* by V_{CC} but by the collector-base voltage V_{CB}. It is clear that V_{CB} forward biases the base-emitter junction and hence base current I_B flows through R_B. This causes the zero signal collector current to flow in the circuit.

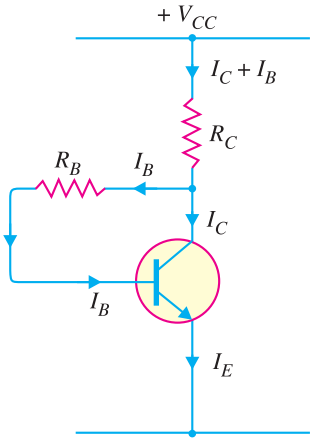


Fig. 9.19

Circuit analysis. The required value of R_B needed to give the zero signal current I_C can be determined as follows. Referring to Fig. 9.19,

$$V_{CC} = {}^*I_C R_C + I_B R_B + V_{BE}$$

$$\text{or} \quad R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B}$$

$$= \frac{V_{CC} - V_{BE} - \beta\, I_B R_C}{I_B} \quad (\because I_C = \beta\, I_B)$$

$$\text{Alternatively,} \quad V_{CE} = V_{BE} + V_{CB}$$

$$\text{or} \quad V_{CB} = V_{CE} - V_{BE}$$

$$\therefore \quad R_B = \frac{V_{CB}}{I_B} = \frac{V_{CE} - V_{BE}}{I_B}; \quad \text{where} \quad I_B = \frac{I_C}{\beta}$$

It can be shown mathematically that stability factor S for this method of biasing is less than $(\beta + 1)$ *i.e.*

$$\text{Stability factor, } S < (\beta + 1)$$

Therefore, this method provides better thermal stability than the fixed bias.

Note. It can be easily proved (See **example 9.17) that Q-point values (I_C and V_{CE}) for the circuit shown in Fig. 9.19 are given by ;

$$I_C = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C}$$

$$\text{and} \quad V_{CE} = V_{CC} - I_C R_C$$

Advantages

(i) It is a simple method as it requires only one resistance R_B.

(ii) This circuit provides some stabilisation of the operating point as discussed below :

$$V_{CE} = V_{BE} + V_{CB}$$

* Actually voltage drop across $R_C = (I_B + I_C)\, R_C$.
However, $I_B << I_C$. Therefore, as a reasonable approximation, we can say that drop across $R_C = I_C R_C$.

** Put $R_E = 0$ for the expression of I_C in exmaple 9.17. It is because in the present circuit (Fig. 9.19), there is no R_E.

Suppose the temperature increases. This will increase collector leakage current and hence the total collector current. But as soon as collector current increases, V_{CE} decreases due to greater drop across R_C. The result is that V_{CB} decreases *i.e.* lesser voltage is available across R_B. Hence the base current I_B decreases. The smaller I_B tends to decrease the collector current to original value.

Disadvantages

(i) The circuit does not provide good stabilisation because stability factor is fairly high, though it is lesser than that of fixed bias. Therefore, the operating point does change, although to lesser extent, due to temperature variations and other effects.

(ii) This circuit provides a negative feedback which reduces the gain of the amplifier as explained hereafter. During the positive half-cycle of the signal, the collector current increases. The increased collector current would result in greater voltage drop across R_C. This will reduce the base current and hence collector current.

Example 9.14. *Fig. 9.20 shows a silicon transistor biased by collector feedback resistor method. Determine the operating point. Given that* $\beta = 100$.

Solution. $V_{CC} = 20\text{V}, R_B = 100\ \text{k}\Omega, R_C = 1\text{k}\Omega$

Since it is a silicon transistor, $V_{BE} = 0.7$ V.

Assuming I_B to be in mA and using the relation,

$$R_B = \frac{V_{CC} - V_{BE} - \beta I_B R_C}{I_B}$$

or $100 \times I_B = 20 - 0.7 - 100 \times I_B \times 1$

or $200\ I_B = 19.3$

or $I_B = \frac{19.3}{200} = 0.096$ mA

$\therefore$ Collector current, $I_C = \beta I_B = 100 \times 0.096 = 9.6$ mA

Collector-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C$$
$$= 20 - 9.6\ \text{mA} \times 1\ \text{k}\Omega$$
$$= 10.4\ \text{V}$$

$\therefore$ Operating point is **10.4 V, 9.6 mA.**

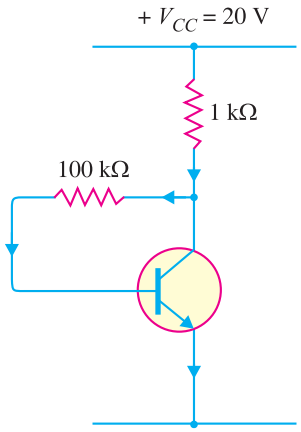


Fig. 9.20

Alternatively

$$I_C = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C} = \frac{20\text{V} - 0.7\text{V}}{100\ \text{k}\Omega/100 + 1\ \text{k}\Omega} = \frac{19.3\text{V}}{2\ \text{k}\Omega} = \mathbf{9.65\ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 20\text{V} - 9.65\ \text{mA} \times 1\ \text{k}\Omega = \mathbf{10.35V}$$

A very slight difference in the values is due to manipulation of calculations.

Example 9.15. *(i) It is required to set the operating point by biasing with collector feedback resistor at* $I_C = 1$*mA,* $V_{CE} = 8$*V. If* $\beta = 100$*,* $V_{CC} = 12$*V,* $V_{BE} = 0.3$*V, how will you do it ?*

(ii) What will be the new operating point if $\beta = 50$*, all other circuit values remaining the same ?*

Solution. $V_{CC} = 12\text{V}, V_{CE} = 8\text{V}, I_C = 1\text{mA}$

$\beta = 100, V_{BE} = 0.3\text{V}$

(i) To obtain the required operating point, we should find the value of R_B.

Now, collector load is

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{(12 - 8)\text{ V}}{1\text{ mA}} = 4\text{ k}\Omega$$

$$\text{Also } I_B = \frac{I_C}{\beta} = \frac{1\text{ mA}}{100} = 0.01\text{ mA}$$

$$\text{Using the relation, } R_B = \frac{V_{CC} - V_{BE} - \beta I_B R_C}{I_B}$$

$$= \frac{12 - 0.3 - 100 \times 0.01 \times 4}{0.01} = \mathbf{770\ k\Omega}$$

(ii) Now $\beta = 50$, and other circuit values remain the same.

$$\therefore \quad V_{CC} = V_{BE} + I_B R_B + \beta I_B R_C$$

$$\text{or} \quad 12 = 0.3 + I_B (R_B + \beta R_C)$$

$$\text{or} \quad 11.7 = I_B (770 + 50 \times 4)$$

$$\text{or} \quad I_B = \frac{11.7\text{ V}}{970\text{ k}\Omega} = 0.012\text{ mA}$$

$$\therefore \quad \text{Collector current, } I_C = \beta I_B = 50 \times 0.012 = 0.6\text{ mA}$$

$$\therefore \quad \text{Collector-emitter voltage, } V_{CE} = V_{CC} - I_C R_C = 12 - 0.6\text{ mA} \times 4\text{ k}\Omega = 9.6\text{ V}$$

$\therefore$ New operating point is **9.6 V, 0.6 mA.**

Comments. It may be seen that operating point is changed when a new transistor with lesser β is used. Therefore, biasing with collector feedback resistor does not provide very good stabilisation. It may be noted, however, that change in operating point is less than that of base resistor method.

Example 9.16. *It is desired to set the operating point at 2V, 1mA by biasing a silicon transistor with collector feedback resistor R_B. If $\beta = 100$, find the value of R_B.*

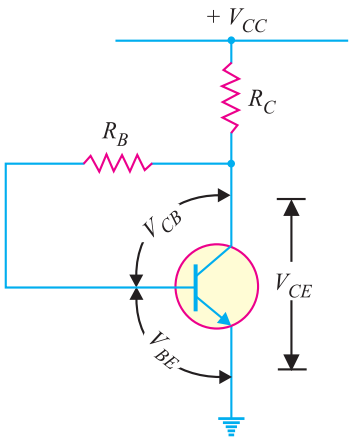


Fig. 9.21

Solution.

For a silicon transistor,

$$V_{BE} = 0.7\text{ V}$$

$$I_B = \frac{I_C}{\beta} = 1/100 = 0.01\text{ mA}$$

$$\text{Now} \quad V_{CE} = V_{BE} + V_{CB}$$

$$\text{or} \quad 2 = 0.7 + V_{CB}$$

$$\therefore \quad V_{CB} = 2 - 0.7 = 1.3\text{ V}$$

$$\therefore \quad R_B = \frac{V_{CB}}{I_B} = \frac{1.3\text{V}}{0.01\text{ mA}} = \mathbf{130\ k\Omega}$$

Example 9.17. *Find the Q-point values (I_C and V_{CE}) for the collector feedback bias circuit shown in Fig. 9.22.*

Solution. Fig. 9.22 shows the currents in the three resistors (R_C, R_B and R_E) in the circuit. By following the path through V_{CC}, R_C, R_B, V_{BE} and R_E and applying Kirchhoff's voltage law, we have,

$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

Now $I_B + I_C \simeq I_C$; $I_E \simeq I_C$ and $I_B = \dfrac{I_C}{\beta}$

$\therefore \quad V_{CC} - I_C R_C - \dfrac{I_C}{\beta} R_B - V_{BE} - I_C R_E = 0$

or $\quad I_C \left(R_E + \dfrac{R_B}{\beta} + R_C\right) = V_{CC} - V_{BE}$

$\therefore \quad I_C = \dfrac{V_{CC} - V_{BE}}{R_E + R_B/\beta + R_C}$

Putting the given circuit values, we have,

$$I_C = \frac{12\text{V} - 0.7\text{V}}{1\ \text{k}\Omega + 400\ \text{k}\Omega/100 + 4\ \text{k}\Omega}$$

$$= \frac{11.3\text{V}}{9\ \text{k}\Omega} = 1.26\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 12\text{V} - 1.26\ \text{mA}\ (4\text{k}\Omega + 1\ \text{k}\Omega)$$

$$= 12\text{V} - 6.3\text{V} = 5.7\text{V}$$

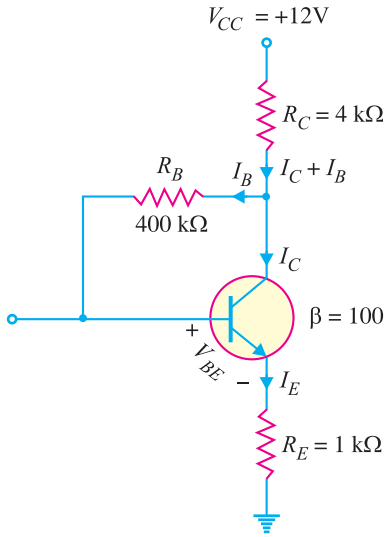


Fig. 9.22

$\therefore$ The operating point is **5.7V, 1.26 mA.**

Example 9.18. *Find the d.c. bias values for the collector-feedback biasing circuit shown in Fig. 9.23. How does the circuit maintain a stable Q point against temperature variations ?*

Solution. The collector current is

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta + R_C}$$

$$= \frac{10\text{V} - 0.7\text{V}}{0 + 100\ \text{k}\Omega/100 + 10\ \text{k}\Omega}$$

$$= \frac{9.3\text{V}}{11\ \text{k}\Omega} = 0.845\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 10\text{V} - 0.845\ \text{mA} \times 10\ \text{k}\Omega$$

$$= 10\text{V} - 8.45\ \text{V} = 1.55\text{V}$$

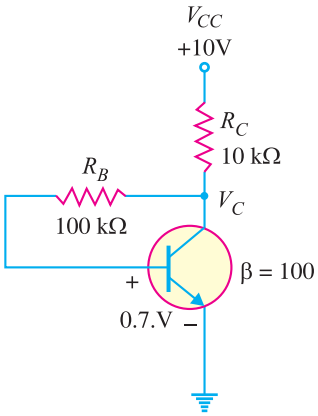


Fig. 9.23

$\therefore$ Operating point is **1.55V, 0.845 mA.**

Stability of Q-point. We know that β varies directly with temperature and V_{BE} varies inversely with temperature. As the temperature goes up, β goes up and V_{BE} goes down. The increase in β increases I_C (= βI_B). The decrease in V_{BE} increases I_B which in turn increases I_C. As I_C tries to increase, the voltage drop across R_C (= $I_C R_C$) also tries to increases. This tends to reduce collector voltage V_C (See Fig. 9.23) and, therefore, the voltage across R_B. The reduced voltage across R_B reduces I_B and offsets the attempted increase in I_C and attempted decrease in V_C. The result is that the collector-feedback circuit maintains a stable Q-point. The reverse action occurs when the temperature decreases.

9.12 Voltage Divider Bias Method

This is the most widely used method of providing biasing and stabilisation to a transistor. In this method, two resistances R_1 and R_2 are connected across the supply voltage V_{CC} (See Fig. 9.24) and provide biasing. The emitter resistance R_E provides stabilisation. The name "voltage divider" comes from the voltage divider formed by R_1 and R_2. The voltage drop across R_2 forward biases the base-

emitter junction. This causes the base current and hence collector current flow in the zero signal conditions.

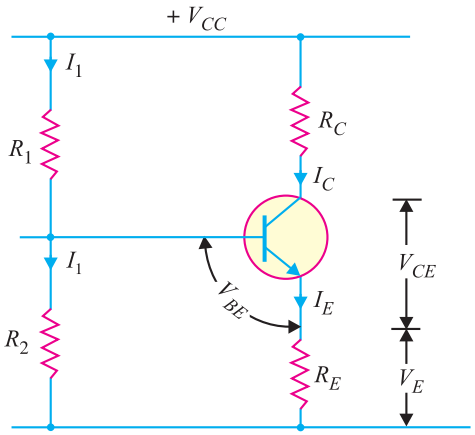


Fig. 9.24

Circuit analysis. Suppose that the current flowing through resistance R_1 is I_1. As base current I_B is very small, therefore, it can be assumed with reasonable accuracy that current flowing through R_2 is also I_1.

(*i*) Collector current I_C :

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$\therefore$ Voltage across resistance R_2 is

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$$

Applying Kirchhoff's voltage law to the base circuit of Fig. 9.24,

$$V_2 = V_{BE} + V_E$$

or $$V_2 = V_{BE} + I_E R_E$$

or $$I_E = \frac{V_2 - V_{BE}}{R_E}$$

Since $I_E \simeq I_C$

$\therefore$ $$I_C = \frac{V_2 - V_{BE}}{R_E} \quad ...(i)$$

It is clear from exp. (*i*) above that I_C does not at all depend upon β. Though I_C depends upon V_{BE} but in practice $V_2 >> V_{BE}$ so that I_C is practically independent of V_{BE}. Thus I_C in this circuit is almost independent of transistor parameters and hence good stabilisation is ensured. It is due to this reason that potential divider bias has become universal method for providing transistor biasing.

(*ii*) Collector-emitter voltage V_{CE}. Applying Kirchhoff's voltage law to the collector side,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$= I_C R_C + V_{CE} + I_C R_E \qquad (\because I_E \simeq I_C)$$

$$= I_C (R_C + R_E) + V_{CE}$$

$$\therefore \quad V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Stabilisation. In this circuit, excellent stabilisation is provided by R_E. Consideration of eq. (*i*) reveals this fact.

$$V_2 = V_{BE} + I_C R_E$$

Suppose the collector current I_C increases due to rise in temperature. This will cause the voltage drop across emitter resistance R_E to increase. As voltage drop across R_2 (*i.e.* V_2) is *independent of I_C, therefore, V_{BE} decreases. This in turn causes I_B to decrease. The reduced value of I_B tends to restore I_C to the original value.

Stability factor. It can be shown mathematically (See Art. 9.13) that stability factor of the circuit is given by :

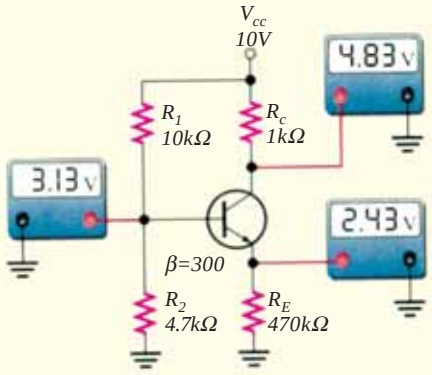
$$\text{Stability factor, } S = \frac{(\beta + 1)(R_0 + R_E)}{R_0 + R_E + \beta R_E}$$

$$= (\beta + 1) \times \frac{1 + \dfrac{R_0}{R_E}}{\beta + 1 + \dfrac{R_0}{R_E}}$$

$$\text{where } R_0 = \frac{R_1 R_2}{R_1 + R_2}$$

If the ratio R_0/R_E is very small, then R_0/R_E can be neglected as compared to 1 and the stability factor becomes :

$$\text{Stability factor} = (\beta + 1) \times \frac{1}{\beta + 1} = 1$$



A voltage divider biased transistor with correct voltages

This is the smallest possible value of S and leads to the maximum possible thermal stability. Due to design **considerations, R_0 / R_E has a value that cannot be neglected as compared to 1. In actual practice, the circuit may have stability factor around 10.

Example 9.19. *Fig. 9.25 (i) shows the voltage divider bias method. Draw the d.c. load line and determine the operating point. Assume the transistor to be of silicon.*

Solution.

d.c. load line. The collector-emitter voltage V_{CE} is given by :

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

When $I_C = 0$, $V_{CE} = V_{CC} = 15$V. This locates the first point B ($OB = 15$V) of the load line on the collector-emitter voltage axis.

$$\text{When } V_{CE} = 0, \quad I_C = \frac{V_{CC}}{R_C + R_E} = \frac{15 \text{ V}}{(1 + 2)\text{ k}\Omega} = 5 \text{ mA}$$

This locates the second point A ($OA = 5$ mA) of the load line on the collector current axis. By joining points A and B, the d.c. load line AB is constructed as shown in Fig. 9.25 (*ii*).

* Voltage drop across $R_2 = \left(\dfrac{V_{CC}}{R_1 + R_2}\right) R_2$

** Low value of R_0 can be obtained by making R_2 very small. But with low value of R_2, current drawn from V_{CC} will be large. This puts restrictions on the choice of R_0. Increasing the value of R_E requires greater V_{CC} in order to maintain the same value of zero signal collector current. Therefore, the ratio R_0/R_E cannot be made very small from design point of view.

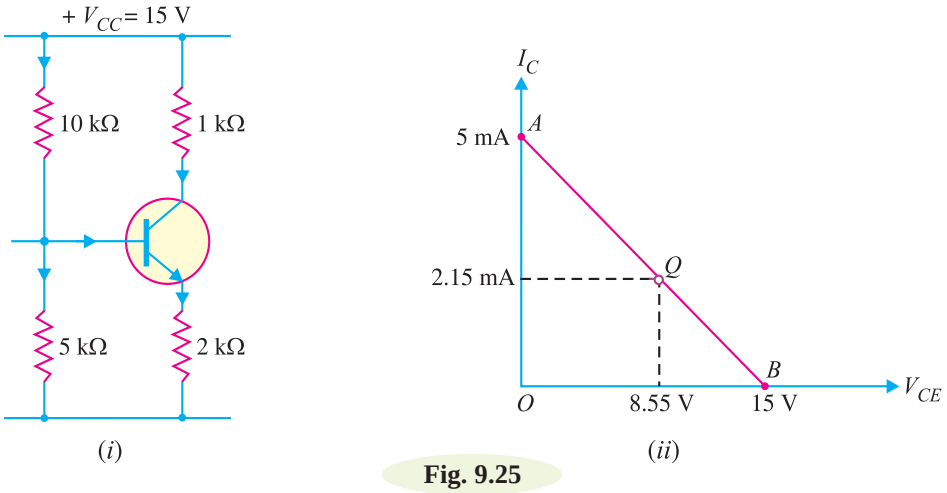


Fig. 9.25

Operating point. For silicon transistor,

$$V_{BE} = 0.7 \text{ V}$$

Voltage across 5 kΩ is

$$V_2 = \frac{V_{CC}}{10+5} \times 5 = \frac{15 \times 5}{10+5} = 5 \text{ V}$$

$$\therefore \quad \text{Emitter current, } I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{5 - 0.7}{2 \text{ k}\Omega} = \frac{4.3 \text{ V}}{2 \text{ k}\Omega} = 2.15 \text{ mA}$$

$\therefore$ Collector current is

$$I_C \simeq I_E = 2.15 \text{ mA}$$

$$\text{Collector-emitter voltage, } V_{CE} = V_{CC} - I_C (R_C + R_E)$$
$$= 15 - 2.15 \text{ mA} \times 3 \text{ k}\Omega = 15 - 6.45 = 8.55 \text{ V}$$

$\therefore$ Operating point is **8.55 V, 2.15 mA.**

Fig.9.25 (*ii*) shows the operating point *Q* on the load line. Its co-ordinates are $I_C = 2.15$ mA, $V_{CE} = 8.55$ V.

Example 9.20. *Determine the operating point of the circuit shown in the previous problem by using Thevenin's theorem.*

Solution. The circuit is redrawn and shown in Fig. 9.26 (*i*) for facility of reference. The d.c. circuit to the left of base terminal *B* can be replaced by Thevenin's equivalent circuit shown in Fig. 9.26 (*ii*). Looking to the left from the base terminal *B* [See Fig. 9.26 (*i*)], Thevenin's equivalent voltage E_0 is given by :

$$E_0 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2 = \left(\frac{15}{10+5}\right) \times 5 = 5 \text{ V}$$

Again looking to the left from the base terminal *B* [See Fig. 9.26 (*i*)], Thevenin's equivalent resistance R_0 is given by :

$$R_0 = \frac{R_1 R_2}{R_1 + R_2}$$

Fig. 9.26 (*ii*) shows the replacement of bias portion of the circuit of Fig. 9.26 (*i*) by its Thevenin's equivalent.

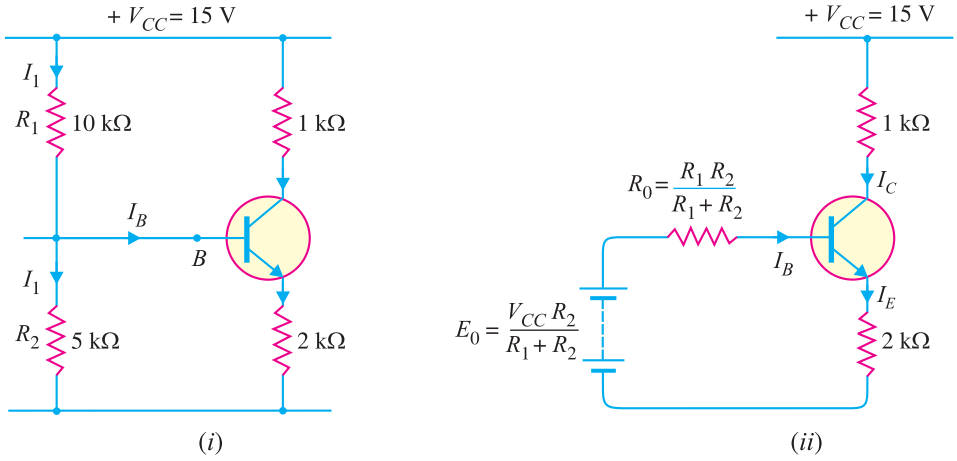


Fig. 9.26

Referring to Fig. 9.26 (*ii*), we have,

$$E_0 = I_B R_0 + V_{BE} + I_E R_E = I_B R_0 + V_{BE} + I_C R_E \qquad (\because I_E \simeq I_C)$$
$$= I_B R_0 + V_{BE} + \beta I_B R_E = I_B (R_0 + \beta R_E) + V_{BE}$$

or $$I_B = \frac{E_0 - V_{BE}}{R_0 + \beta R_E}$$

$\therefore$ Collector current, $$I_C = \beta I_B = \frac{\beta (E_0 - V_{BE})}{R_0 + \beta R_E}$$

Dividing the numerator and denominator of R.H.S. by β, we get,

$$I_C = \frac{E_0 - V_{BE}}{\frac{R_0}{\beta} + R_E}$$

As *$R_0 / \beta << R_E$, therefore, R_0/β may be neglected as compared to R_E.

$$\therefore \quad I_C = \frac{E_0 - V_{BE}}{R_E} = \frac{5 - 0.7}{2\ \text{k}\Omega} = 2.15\ \text{mA}$$
$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 15 - 2.15\ \text{mA} \times 3\ \text{k}\Omega$$
$$= 15 - 6.45 = 8.55\ \text{V}$$

$\therefore$ Operating point is **8.55 V, 2.15 mA.**

Example 9.21. *A transistor uses potential divider method of biasing. R_1 = 50 kΩ, R_2 = 10 kΩ and R_E = 1kΩ. If V_{CC} = 12 V, find :*

(i) the value of I_C ; given V_{BE} = 0.1V

(ii) the value of I_C ; given V_{BE} = 0.3V. Comment on the result.

Solution. $R_1 = 50\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$, $R_E = 1\ \text{k}\Omega$, $V_{CC} = 12\ \text{V}$

(*i*) When $V_{BE} = 0.1$ V,

$$\text{Voltage across } R_2,\ V_2 = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{10}{50 + 10} \times 12 = 2\ \text{V}$$

$$\therefore \quad \text{Collector current, } I_C = \frac{V_2 - V_{BE}}{R_E} = \frac{2 - 0.1}{1\ \text{k}\Omega} = \mathbf{1.9\ mA}$$

* In fact, this condition means that I_B is very small as compared to I_1, the current flowing through R_1 and R_2.

(ii) When $V_{BE} = 0.3$ V,

$$\text{Collector current, } I_C = \frac{V_2 - V_{BE}}{R_E} = \frac{2 - 0.3}{1\ \text{k}\Omega} = \mathbf{1.7\ mA}$$

Comments. From the above example, it is clear that although V_{BE} varies by 300%, the value of I_C changes only by nearly 10%. This explains that in this method, I_C is almost independent of transistor parameter variations.

Example 9.22. *Calculate the emitter current in the voltage divider circuit shown in Fig. 9.27. Also find the value of V_{CE} and collector potential V_C.*

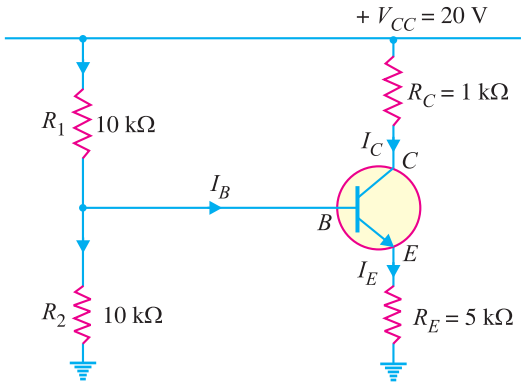


Fig. 9.27

Solution.

$$\text{Voltage across } R_2,\ V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2 = \left(\frac{20}{10 + 10}\right) 10 = 10\ \text{V}$$

Now $V_2 = V_{BE} + I_E R_E$

As V_{BE} is generally small, therefore, it can be neglected.

$$\therefore \quad I_E = \frac{V_2}{R_E} = \frac{10\ \text{V}}{5\ \text{k}\Omega} = \mathbf{2\ mA}$$

Now $I_C \simeq I_E = 2$ mA

$$\therefore \quad V_{CE} = V_{CC} - I_C (R_C + R_E) = 20 - 2\ \text{mA}\ (6\ \text{k}\Omega)$$
$$= 20 - 12 = \mathbf{8\ V}$$

$$\text{Collector potential, } V_C = V_{CC} - I_C R_C = 20 - 2\ \text{mA} \times 1\ \text{k}\Omega$$
$$= 20 - 2 = \mathbf{18\ V}$$

9.13 Stability Factor For Potential Divider Bias

We have already seen (See example 9.20) how to replace the potential divider circuit of potential divider bias by Thevenin's equivalent circuit. The resulting potential divider bias circuit is redrawn in Fig. 9.28 in order to find the stability factor S for this biasing circuit. Referring to Fig. 9.28 and applying Kirchhoff's voltage law to the base circuit, we have,

$$E_0 - I_B R_0 - V_{BE} - I_E R_E = 0$$

or $$E_0 = I_B R_0 + V_{BE} + (I_B + I_C) R_E$$

Considering V_{BE} to be constant and differentiating the above equation w.r.t. I_C, we have,

$$0 = R_0 \frac{dI_B}{dI_C} + 0 + R_E \frac{dI_B}{dI_C} + R_E$$

or $$0 = \frac{dI_B}{dI_C}(R_0 + R_E) + R_E$$

$$\therefore \quad \frac{dI_B}{dI_C} = \frac{-R_E}{R_0 + R_E} \qquad ...(i)$$

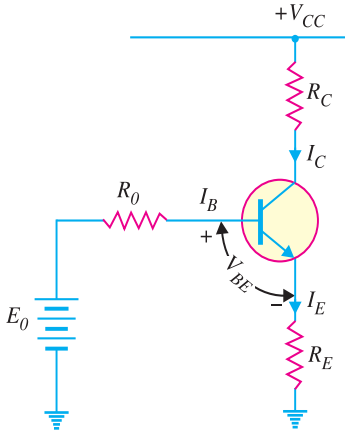


Fig. 9.28

The general expression for stability factor is

$$\text{Stability factor, } S = \frac{\beta + 1}{1 - \beta \dfrac{dI_B}{dI_C}}$$

Putting the value of dI_B/dI_C from eq. (i) into the expression for S, we have,

$$S = \frac{\beta + 1}{1 - \beta \dfrac{-R_E}{R_0 + R_E}} = \frac{\beta + 1}{1 + \left(\dfrac{\beta R_E}{R_0 + R_E}\right)}$$

$$= \frac{(\beta + 1)(R_0 + R_E)}{R_0 + R_E + \beta R_E} = \frac{(\beta + 1)(R_0 + R_E)}{R_0 + R_E(\beta + 1)}$$

$$\therefore \quad S = (\beta + 1) \times \frac{R_0 + R_E}{R_E(\beta + 1) + R_0}$$

Dividing the numerator and denominator of R.H.S. of the above equation by R_E, we have,

$$S = (\beta + 1) \times \frac{1 + R_0/R_E}{\beta + 1 + R_0/R_E} \qquad ...(ii)$$

Eq. (ii) gives the formula for the stability factor S for the potential divider bias circuit. The following points may be noted carefully :

(i) For greater thermal stability, the value of S should be small. This can be achieved by making R_0/R_E small. If R_0/R_E is made very small, then it can be neglected as compared to 1.

$$\therefore \quad S = (\beta + 1) \times \frac{1}{\beta + 1} = 1$$

This is the ideal value of S and leads to the maximum thermal stability.

(ii) The ratio *R_0/R_E can be made very small by decreasing R_0 and increasing R_E. Low value of

* Remember, R_0 = Thevenin's equivalent resistance = $\dfrac{R_1 R_2}{R_1 + R_2}$

R_0 can be obtained by making R_2 very small. But with low value of R_2, current drawn from V_{CC} will be large. This puts restriction on the choice of R_0. Increasing the value of R_E requires greater V_{CC} in order to maintain the same zero signal collector current. Due to these limitations, a compromise is made in the selection of the values of R_0 and R_E. Generally, these values are so selected that $S \simeq 10$.

Example 9.23. *For the circuit shown in Fig. 9.29 (i), find the operating point. What is the stability factor of the circuit ? Given that $\beta = 50$ and $V_{BE} = 0.7V$.*

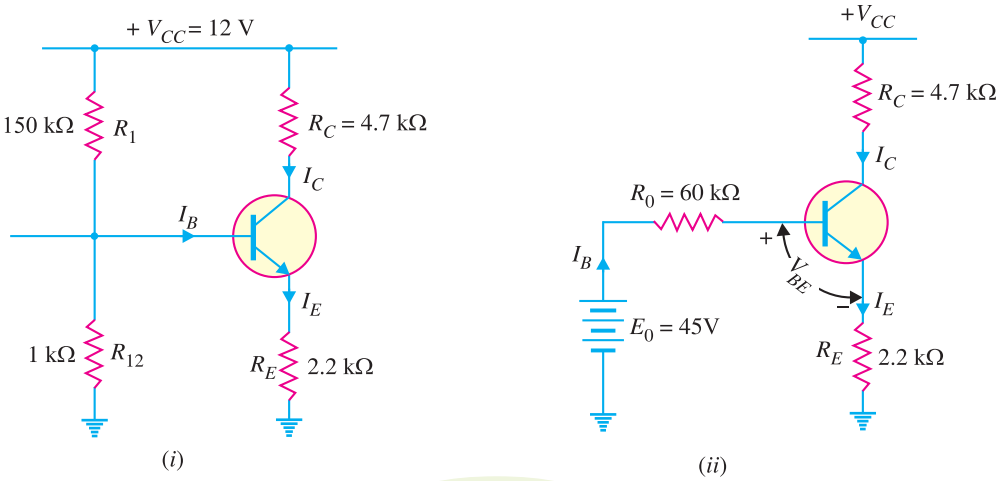


Fig. 9.29

Solution. Fig. 9.29 (*i*) shows the circuit of potential divider bias whereas Fig. 9.29 (*ii*) shows it with potential divider circuit replaced by Thevenin's equivalent circuit.

$$E_0 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{12V}{150\ k\Omega + 100\ k\Omega} \times 100\ k\Omega = 4.8V$$

$$R_0 = \frac{R_1 R_2}{R_1 + R_2} = \frac{150\ k\Omega \times 100\ k\Omega}{150\ k\Omega + 100\ k\Omega} = 60\ k\Omega$$

$$\therefore \quad I_B = \frac{E_0 - V_{BE}}{R_0 + \beta R_E} \qquad \text{..... (See Ex. 9.20)}$$

$$= \frac{4.8V - 0.7V}{60\ k\Omega + 50 \times 2.2\ k\Omega} = \frac{4.1V}{170\ k\Omega} = 0.024\ mA$$

Now $I_C = \beta I_B = 50 \times 0.024 = 1.2\ mA$

$\therefore$ $V_{CE} = V_{CC} - I_C (R_C + R_E)$

$= 12V - 1.2mA\ (4.7\ k\Omega + 2.2\ k\Omega) = 3.72V$

$\therefore$ Operating point is **3.72V, 1.2 mA.**

Now $\frac{R_0}{R_E} = \frac{60\ k\Omega}{2.2\ k\Omega} = 27.3$

$\therefore$ Stability factor, $S = (\beta + 1) \times \frac{1 + R_0 / R_E}{\beta + 1 + R_0 / R_E}$

$= (50 + 1) \times \frac{1 + 27.3}{50 + 1 + 27.3} =$ **18.4**

Note. We can also find the value of I_C and V_{CE} (See Art. 9.12) as under :

$$I_C = \frac{V_2 - V_{BE}}{R_E} \quad \text{where } V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2$$

and $V_{CE} = V_{CC} - I_C (R_C + R_E)$

However, by replacing the potential divider circuit by Thevenin's equivalent circuit, the expression for I_C can be found more accurately. If not mentioned in the problem, any one of the two methods can be used to obtain the solution.

Example 9.24. *The circuit shown in Fig. 9.30 (i) uses silicon transistor having $\beta = 100$. Find the operating point and stability factor.*

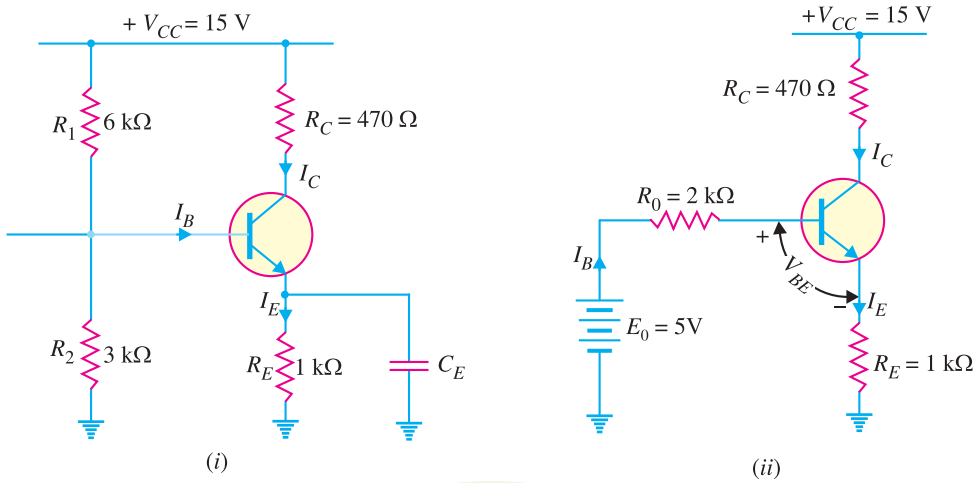


Fig 9.30

Solution. Fig. 9.30 (*i*) shows the circuit of potential divider bias whereas Fig. 9.30 (*ii*) shows it with potential divider circuit replaced by Thevenin's equivalent circuit.

$$E_0 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{15\text{V}}{6\ \text{k}\Omega + 3\ \text{k}\Omega} \times 3\ \text{k}\Omega = \frac{15\text{V}}{9\ \text{k}\Omega} \times 3\ \text{k}\Omega = 5\text{V}$$

$$R_0 = \frac{R_1 R_2}{R_1 + R_2} = \frac{6\ \text{k}\Omega \times 3\ \text{k}\Omega}{6\ \text{k}\Omega + 3\ \text{k}\Omega} = 2\ \text{k}\Omega$$

Now $$I_B = \frac{E_0 - V_{BE}}{R_0 + \beta R_E}$$

$$= \frac{5\text{V} - 0.7\text{V}}{2\ \text{k}\Omega + 100 \times 1\text{k}\Omega} = \frac{4.3\text{V}}{102\ \text{k}\Omega} = 0.042\text{mA}$$

$\therefore$ $I_C = \beta I_B = 100 \times 0.042 = 4.2$ mA

and $V_{CE} = V_{CC} - I_C (R_C + R_E)$

$= 15\text{V} - 4.2\text{mA}\ (470\Omega + 1\ \text{k}\Omega) = 8.83\text{V}$

$\therefore$ Operating point is **8.83V ; 4.2 mA.**

Now $R_0 / R_E = 2\ \text{k}\Omega / 1\ \text{k}\Omega = 2$

$\therefore$ Stability factor, $S = (\beta + 1) \times \frac{1 + R_0 / R_E}{\beta + 1 + R_0 / R_E}$

$= (100 + 1) \times \frac{1 + 2}{100 + 1 + 2} = \mathbf{2.94}$

9.14 Design of Transistor Biasing Circuits

(For low powered transistors)

In practice, the following steps are taken to design transistor biasing and stabilisation circuits :

Step 1. It is a common practice to take $R_E = 500 - 1000\Omega$. Greater the value of R_E, better is the stabilisation. However, if R_E is very large, higher voltage drop across it leaves reduced voltage drop across the collector load. Consequently, the output is decreased. Therefore, a compromise has to be made in the selection of the value of R_E.

Step 2. The zero signal current I_C is chosen according to the signal swing. However, in the initial stages of most transistor amplifiers, zero signal $I_C = 1$mA is sufficient. The major advantages of selecting this value are :

(i) The output impedance of a transistor is very high at 1mA. This increases the voltage gain.

(ii) There is little danger of overheating as 1mA is quite a small collector current.

It may be noted here that working the transistor below zero signal $I_C = 1$mA is not advisable because of strongly non-linear transistor characteristics.

Step 3. The values of resistances R_1 and R_2 are so selected that current I_1 flowing through R_1 and R_2 is atleast 10 times I_B *i.e.* $I_1 \geq 10\, I_B$. When this condition is satisfied, good stabilisation is achieved.

Step 4. The zero signal I_C should be a little more (say 20%) than the maximum collector current swing due to signal. For example, if collector current change is expected to be 3mA due to signal, then select zero signal $I_C \simeq 3.5$ mA. It is important to note this point. Selecting zero signal I_C below this value may cut off a part of negative half-cycle of a signal. On the other hand, selecting a value much above this value (say 15mA) may unnecessarily overheat the transistor, resulting in wastage of battery power. Moreover, a higher zero signal I_C will reduce the value of R_C (for same V_{CC}), resulting in reduced voltage gain.

Example 9.25. *In the circuit shown in Fig. 9.31, the operating point is chosen such that I_C = 2mA, V_{CE} = 3V. If R_C = 2.2 kΩ, V_{CC} = 9V and β = 50, determine the values of R_1, R_2 and R_E. Take V_{BE} = 0.3V and $I_1 = 10 I_B$.*

Solution. $R_C = 2.2\,\text{k}\Omega$, $V_{CC} = 9\text{V}$, $\beta = 50$

$V_{BE} = 0.3\text{ V}$, $I_1 = 10\, I_B$

As I_B is very small as compared to I_1, therefore, we can assume with reasonable accuracy that I_1 flowing through R_1 also flows through R_2.

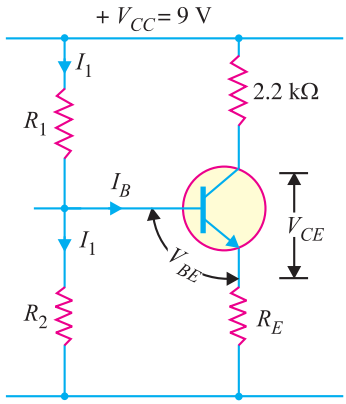


Fig. 9.31

$$\text{Base current, } I_B = \frac{I_C}{\beta} = \frac{2\ mA}{50} = 0.04\text{ mA}$$

Current through R_1 & R_2 is

$$I_1 = 10\, I_B = 10 \times 0.04 = 0.4\text{ mA}$$

Now $$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$$\therefore \quad R_1 + R_2 = \frac{V_{CC}}{I_1} = \frac{9\text{ V}}{0.4\text{ mA}} = 22.5\,\text{k}\Omega$$

Applying Kirchhoff's voltage law to the collector side of the circuit, we get,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

or $V_{CC} = I_C R_C + V_{CE} + I_C R_E$ $(\because I_C \simeq I_E)$

or $9 = 2\text{ mA} \times 2.2\text{ k}\Omega + 3 + 2\text{ mA} \times R_E$

$\therefore \quad R_E = \dfrac{9 - 4.4 - 3}{2} = 0.8\text{ k}\Omega = \mathbf{800\ \Omega}$

Voltage across R_2, $V_2 = V_{BE} + V_E = 0.3 + 2\text{ mA} \times 0.8\text{ k}\Omega$
$= 0.3 + 1.6 = 1.9\text{ V}$

$\therefore$ Resistance $R_2 = V_2/I_1 = 1.9\text{ V}/0.4\text{ mA} = \mathbf{4.75\ k\Omega}$

and $R_1 = 22.5 - 4.75 = \mathbf{17.75\ k\Omega}$

Example 9.26. *An npn transistor circuit (See Fig. 9.32) has $\alpha = 0.985$ and $V_{BE} = 0.3$V. If $V_{CC} = 16$V, calculate R_1 and R_C to place Q point at $I_C = 2$mA, $V_{CE} = 6$ volts.*

Solution. $\alpha = 0.985, \quad V_{BE} = 0.3\text{ V}, \quad V_{CC} = 16\text{ V}$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.985}{1 - 0.985} = 66$$

Base current, $I_B = \dfrac{I_C}{\beta} = \dfrac{2\text{ mA}}{66} = 0.03\text{ mA}$

Voltage across R_2, $V_2 = V_{BE} + V_E = 0.3 + 2\text{ mA} \times 2\text{ k}\Omega$
$= 4.3\text{ V}$

$\therefore$ Voltage across $R_1 = V_{CC} - V_2 = 16 - 4.3 = 11.7\text{ V}$

$\therefore$ Current through R_1 & R_2 is

$$I_1 = \frac{V_2}{R_2} = \frac{4.3\text{ V}}{20\text{ k}\Omega} = 0.215\text{ mA}$$

$\therefore$ Resistance $R_1 = \dfrac{\text{Voltage across } R_1}{I_1} = \dfrac{11.7\text{ V}}{0.215\text{ mA}}$

$= \mathbf{54.4\ k\Omega}$

Voltage across $R_C = V_{CC} - V_{CE} - V_E$
$= 16 - 6 - 2 \times 2 = 6\text{ V}$

$\therefore$ Collector resistance, $R_C = \dfrac{\text{Voltage across } R_C}{I_C} = \dfrac{6\text{ V}}{2\text{ mA}} = \mathbf{3\ k\Omega}$

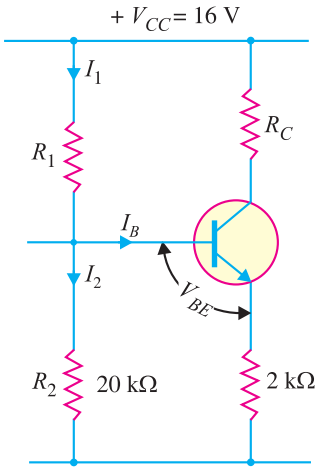


Fig. 9.32

Example 9.27. *Calculate the exact value of emitter current in the circuit shown in Fig. 9.33 (i). Assume the transistor to be of silicon and $\beta = 100$.*

Solution. In order to obtain accurate value of emitter current I_E, we shall replace the bias portion of the circuit shown in Fig. 9.33 (*i*) by its Thevenin's equivalent. Fig. 9.33 (*ii*) shows the desired circuit.

Looking from the base terminal B to the left, Thevenin's voltage E_0 is given by :

$$E_0 = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5}{10 + 5} \times 15 = 5\text{ V}$$

Again looking from the base terminal B to the left, Thevenin's resistance R_0 is given by;

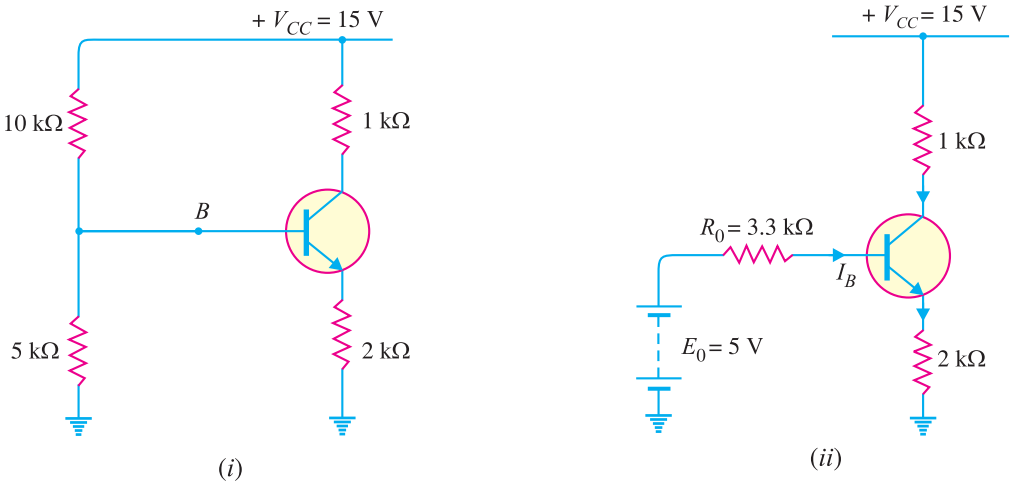


Fig. 9.33

$$R_0 = \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \times 5}{10 + 5} = \frac{50}{15} = 3.3 \text{ k}\Omega$$

Applying Kirchhoff's voltage law to the base-emitter loop [See Fig. 9.33 (*ii*)],

$$E_0 = I_B R_0 + V_{BE} + I_E R_E$$

Since $I_E \simeq I_C$, therefore, $I_B = I_E / \beta$.

$$\therefore \quad E_0 = \frac{I_E}{\beta} R_0 + V_{BE} + I_E R_E$$

$$= I_E \left(\frac{R_0}{\beta} + R_E \right) + V_{BE}$$

$$\therefore \quad I_E = \frac{E_0 - V_{BE}}{\frac{R_0}{\beta} + R_E} = \frac{5 - 0.7}{\frac{3.3}{100} + 2} \qquad \text{(For } Si \text{ transistor, } V_{BE} = 0.7\text{V)}$$

$$= \frac{4.3 \text{ V}}{2.033 \text{ k}\Omega} = \mathbf{2.11 \text{ mA}}$$

Example 9.28. *The potential divider circuit shown in Fig. 9.34 has the values as follows: I_E = 2mA, I_B = 50μA, V_{BE} = 0.2V, R_E = 1kΩ, R_2 = 10 kΩ and V_{CC} = 10V. Find the value of R_1.*

Solution. In this problem, we shall consider that currents through R_1 and R_2 are different, although in practice this difference is very small.

Voltage across R_2, $V_2 = V_{BE} + I_E R_E = 0.2 + 2 \text{ mA} \times 1 \text{ k}\Omega$

$$= 0.2 + 2 = 2.2 \text{ V}$$

Current through R_2, $I_2 = \frac{V_2}{R_2} = \frac{2.2 \text{ V}}{10 \text{ k}\Omega} = 0.22 \text{ mA}$

Current through R_1, $I_1 = I_2 + I_B = 0.22 + 0.05 = 0.27 \text{ mA}$

Voltage across R_1, $V_1 = V_{CC} - V_2 = 10 - 2.2 = 7.8 \text{ V}$

$$\therefore \quad R_1 = \frac{V_1}{I_1} = \frac{7.8 \text{ V}}{0.27 \text{ mA}} = \mathbf{28.89 \text{ k}\Omega}$$

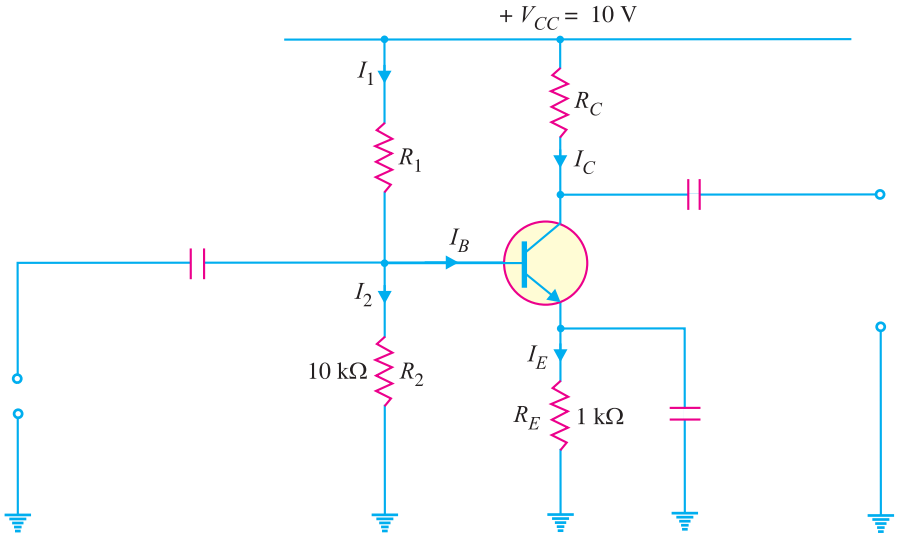


Fig. 9.34

Example 9.29. *Fig. 9.35 shows the potential divider method of biasing. What will happen if*

(*i*) *resistance R_2 is shorted* (*ii*) *resistance R_2 is open-circuited*

(*iii*) *resistance R_1 is shorted* (*iv*) *resistance R_1 is open ?*

Solution. **(*i*)** If resistance R_2 is shorted, the base will be grounded. It will be left without forward bias and the transistor will be cut off *i.e.*, output will be zero.

(*ii*) If resistance R_2 is open, the forward bias will be very high. The collector current will be very high while collector-emitter voltage will be very low.

(*iii*) If resistance R_1 is shorted, the transistor will be in saturation due to excessive forward bias. The base will be at V_{CC} and emitter will be only slightly below V_{CC}.

(*iv*) If R_1 is open, the transistor will be without forward bias. Hence the transistor will be cut off *i.e.* output will be zero.

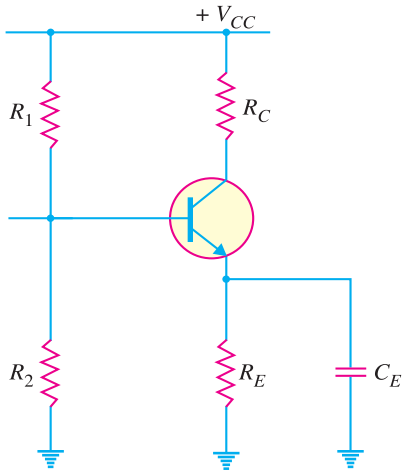


Fig. 9.35

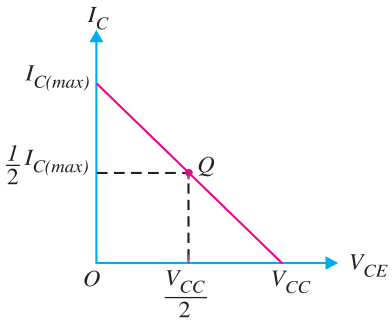


Fig. 9.36

9.15 Mid-Point Biasing

Mid-point biasing

When an amplifier circuit is so designed that operating point Q lies at the centre of d.c. load line, the amplifier is said to be *midpoint biased*. When the amplifier is mid-point biased, the Q-point provides values of I_C and V_{CE} that are one-half of their maximum possible values. This is illustrated in Fig. 9.36. Since the Q-point is centred on the load line;

$$I_C = \frac{1}{2} I_{C\,(max)} \; ; \quad V_{CE} = \frac{V_{CC}}{2}$$

When a transistor is used as an amplifier, it is always designed for mid point bias. The reason is that midpoint biasing allows optimum operation of the amplifier. In other words, midpoint biasing provides the largest possible output. This point is illustrated in Fig. 9.37 where Q-point is centred on the load line.

When an ac signal is applied to the base of the transistor, collector current and collector- emitter voltage will both vary around their Q-point values. Since Q-point is centred, I_C and V_{CE} can both make the maximum possible transitions above and below their initial dc values. If Q-point is located above centre on the load line, the input may cause the transistor to saturate. As a result, a part of the output wave will be clipped off. Similarly, if Q-point is below midpoint on the load line, the input may cause the transistor to go into cut off. This can also cause a portion of the output to be clipped. It follows, therefore, that midpoint biased amplifier circuit allows the best possible ac operation of the circuit.

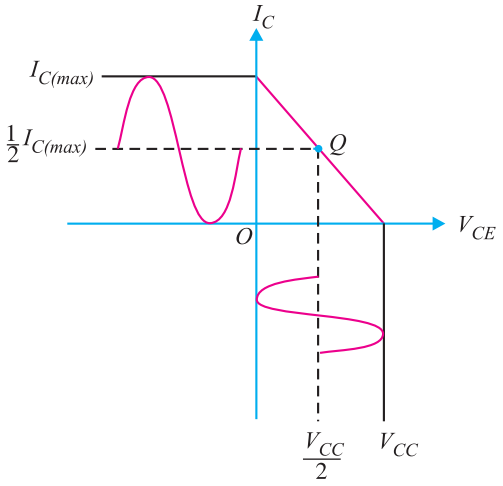


Fig. 9.37

Example 9.30. *Determine whether or not the circuit shown in Fig. 9.38 (i) is midpoint biased.*

Solution. Let us first construct the dc load line.

$$I_{C\,(max)} = \frac{V_{CC}}{R_C} = \frac{8\text{ V}}{2\text{ k}\Omega} = 4\text{ mA}$$

This locates the point A ($OA = 4$ mA) of the dc load line.

$$V_{CE\,(max)} = V_{CC} = 8\text{ V}$$

This locates the point B ($OB = 8$V) of the dc load line. By joining these two points, dc load line AB is constructed [See Fig. 9.38 (ii)].

Operating point. Referring to Fig. 9.38 (i), we have,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{8\text{ V} - 0.7\text{ V}}{360\text{ k}\Omega} = 20.28\ \mu\text{A}$$

$$\therefore \quad I_C = \beta I_B = 100\,(20.28\ \mu\text{A}) = 2.028\text{ mA}$$

Also $$V_{CE} = V_{CC} - I_C R_C = 8\text{ V} - (2.028\text{ mA})\,(2\text{ k}\Omega) = 3.94\text{ V}$$

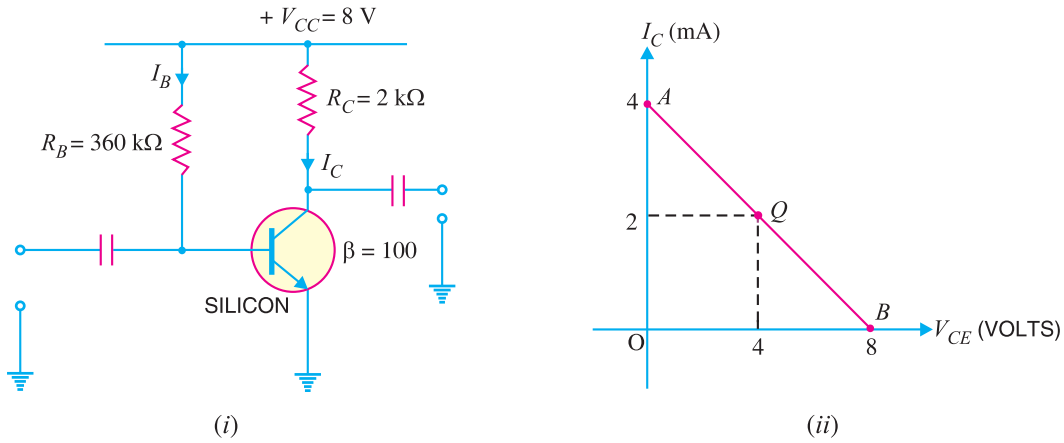


Fig. 9.38

Since V_{CE} is nearly one-half of V_{CC}, *the amplifier circuit is midpoint biased.*

Note. We can determine whether or not the circuit is midpoint biased without drawing the dc load line. By definition, a circuit is midpoint biased when the Q-point value of V_{CE} is one-half of V_{CC}. Therefore, all that you have to do is to find the operating point Q of the circuit. If the Q-point value of V_{CE} is one-half of V_{CC}, the circuit is midpoint biased.

Example 9.31. *Determine whether or not the circuit shown in Fig. 9.39 is midpoint biased.*

Solution. In order to determine whether the circuit is midpoint biased or not, we shall first find the operating point of the circuit.

Voltage across R_2 is

$$V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2$$

$$= \frac{10}{12 + 2.7} \times 2.7 = 1.84 \text{ V}$$

∴ Emitter current is

$$I_E = \frac{V_2 - V_{BE}}{R_E}$$

$$= \frac{1.84 - 0.7}{180} = 6.33 \text{ mA}$$

∴ Collector current is

$$I_C \simeq I_E = \mathbf{6.33\ mA}$$

Collector-emitter voltage is

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 10 - 6.33\ (0.62 + 0.18) = \mathbf{4.94\ V}$$

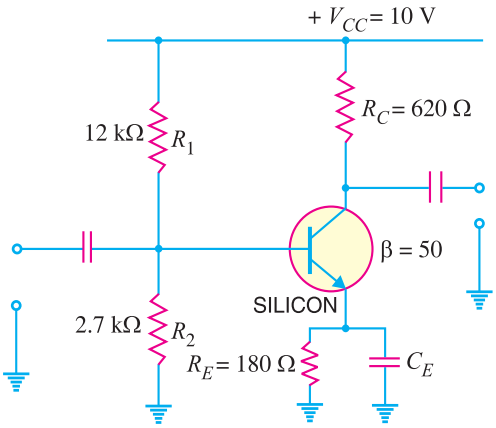


Fig. 9.39

Since Q-point value of V_{CE} is approximately one-half of V_{CC} (= 10 V), *the circuit is midpoint biased.* Note that answer has been obtained without the use of a dc load line.

9.16 Which Value of β to be used ?

While analysing a biasing circuit, we have to refer to the specification sheet for the transistor to obtain the value of β. Normally, the transistor specification sheet lists a minimum value (β_{min}) and maximum value (β_{max}) of β. In that case, the *geometric average of the two values* should be used.

$$\beta_{av} = \sqrt{\beta_{min} \times \beta_{max}}$$

Note. If only one value of β is listed on the specification sheet, we should then use that value.

Example 9.32. *Find the value of I_B for the circuit shown in Fig. 9.40. Given that β has a range of 100 to 400 when I_C = 10 mA.*

Solution. Voltage across R_2 is

$$V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{10}{1.5 + 0.68} \times 0.68 = 3.12 \text{ V}$$

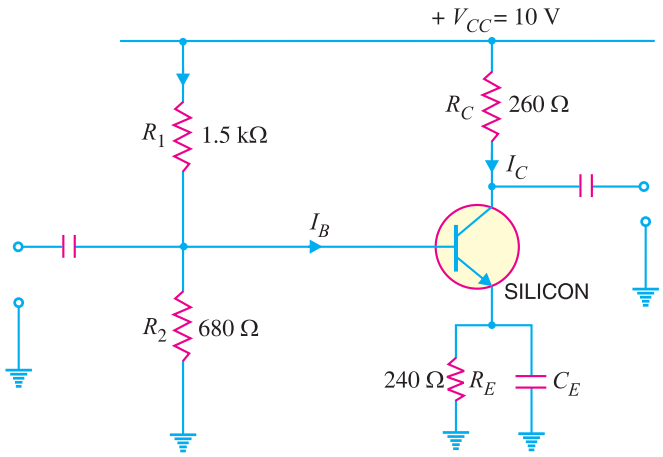


Fig. 9.40

$$\therefore \quad \text{Emitter current, } I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{3.12 - 0.7}{0.24} = 10 \text{ mA}$$

$$\therefore \quad \text{Collector current, } I_C \simeq I_E = 10 \text{ mA}$$

It is given that β has a range of 100 to 400 when *Q*-point value of I_C is 10mA.

$$\therefore \quad \beta_{av} = \sqrt{\beta_{min} \times \beta_{max}} = \sqrt{100 \times 400} = 200$$

$$\therefore \quad \text{Base current, } I_B = \frac{I_E}{\beta_{av} + 1} = \frac{10 \text{ mA}}{200 + 1} = \mathbf{49.75\ \mu A}$$

9.17 Miscellaneous Bias Circuits

In practice, one may find that bias circuits which do not always confirm to the basic forms considered in this chapter. There may be slight circuit modifications. However, such bias circuits should not pose any problem if the basic approach to transistor biasing is understood. We shall solve a few examples to show how the basic concepts of biasing can be applied to any biasing circuit.

Example 9.33. *Calculate the operating point of the circuit shown in Fig. 9.41. Given β = 60 and V_{BE} = 0.7V.*

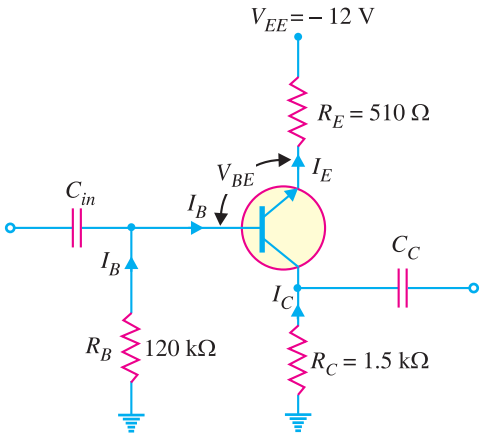


Fig. 9.41

Solution. Such a problem should not pose any difficulty. We are to simply find the d.c. values. Note that capacitors behave as open to d.c. Applying Kirchhoff's voltage law to the path passing through R_B, V_{BE}, R_E and V_{EE}, we have,

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

or $$V_{EE} = I_B R_B + V_{BE} + I_C R_E \quad (\because\ I_E \simeq I_C)$$

or $$V_{EE} - V_{BE} = I_B R_B + \beta I_B R_E \quad (\because\ I_C = \beta I_B)$$

$$\therefore \quad I_B = \frac{V_{EE} - V_{BE}}{R_B + \beta R_E}$$

$$= \frac{12\text{V} - 0.7\text{V}}{120\ \text{k}\Omega + 60 \times 0.510\ \text{k}\Omega} = \frac{11.3\text{V}}{150.6\ \text{k}\Omega} = 0.075\ \text{mA}$$

Now $$I_C = \beta I_B = 60 \times 0.075\ \text{mA} = 4.5\ \text{mA}$$

and $$V_{CE} = V_{EE} - I_C (R_C + R_E)$$

$$= 12\text{V} - 4.5\ \text{mA}\ (1.5\ \text{k}\Omega + 0.510\ \text{k}\Omega) = 2.96\text{V}$$

$\therefore$ Operating point is **2.96V, 4.5 mA.**

Example 9.34. *Find the operating point for the circuit shown in Fig. 9.42. Assume $\beta = 45$ and $V_{BE} = 0.7$V.*

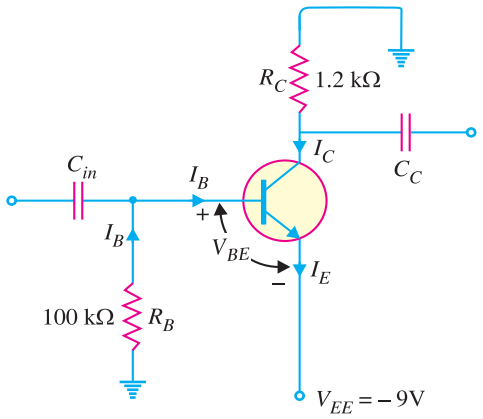


Fig. 9.42

Solution.

$$V_{EE} = I_B R_B + V_{BE}$$

or $$I_B = \frac{V_{EE} - V_{BE}}{R_B} = \frac{(9 - 0.7)\,\text{V}}{100\ \text{k}\Omega} = 0.083\ \text{mA}$$

$\therefore$ $$I_C = \beta I_B = 45 \times 0.083\ \text{mA} = 3.73\ \text{mA}$$

Also $$V_{EE} = I_C R_C + V_{CE}$$

$\therefore$ $$V_{CE} = V_{EE} - I_C R_C = 9\text{V} - (3.\ 73\ \text{mA})\ (1.2\ \text{k}\Omega) = 4.52\text{V}$$

$\therefore$ Operating point is **4.52V, 3.73 mA.**

Example 9.35. *It is desired to design the biasing circuit of an amplifier in Fig. 9.43 in such a way to have an operating point of 6V, 1 mA. If transistor has β = 150, find R_E, R_C, R_1 and R_2. Assume V_{BE} = 0.7V.*

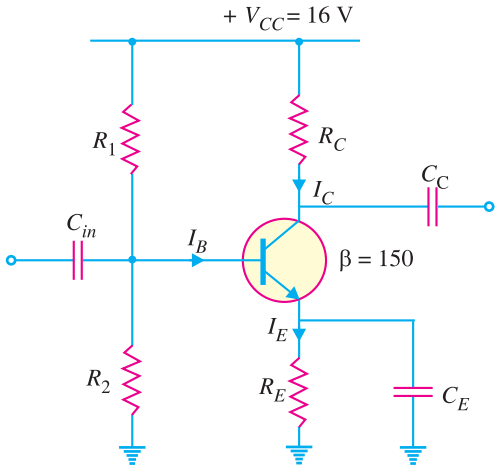


Fig. 9.43

Solution. We are given V_{CC}, β and the operating point. It is desired to find the component values. For good design, voltage across R_E (*i.e.*, V_E) should be one-tenth of V_{CC} *i.e.*

$$V_E = \frac{V_{CC}}{10} = \frac{16\text{V}}{10} = 1.6\text{V}$$

$\therefore$ $$R_E = \frac{V_E}{I_E} = \frac{V_E}{I_C} = \frac{1.6\text{V}}{1\ \text{mA}} = \mathbf{1.6\ k\Omega}$$

Now $$V_{CC} = I_C R_C + V_{CE} + V_E$$

$\therefore$ $$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{16 - 6\text{V} - 1.6\text{V}}{1\ \text{mA}} = \mathbf{8.4\ k\Omega}$$

$$V_2 = V_E + V_{BE} = 1.6 + 0.7 = 2.3\text{V}$$

Now $$R_2 = \frac{1}{10} *(\beta R_E) = \frac{1}{10}\ (150 \times 1.6\ \text{k}\Omega) = \mathbf{24\ k\Omega}$$

Also $$V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2$$

or $$2.3\text{V} = \frac{16\text{V}}{R_1 + 24\ \text{k}\Omega} \times 24\ \text{k}\Omega \qquad \therefore R_1 = \mathbf{143\ k\Omega}$$

* This relation stems from $I_1 = 10\ I_B$.

9.18 Silicon Versus Germanium

Although both silicon and germanium are used in semiconductor devices, the present day trend is to use silicon. The main reasons for this are :

(i) *Smaller I_{CBO}.* At room temperature, a silicon crystal has fewer free electrons than a germanium crystal. This implies that silicon will have much smaller collector cut off current (I_{CBO}) than that of germanium. In general, with germanium, I_{CBO} is 10 to 100 times greater than with silicon. The typical values of I_{CBO} at 25°C (the figures most often used for normal temperature) for small signal transistors are:

Silicon : 0.01 μA to 1μA

Germanium : 2 to 15 μA

(ii) *Smaller variation of I_{CBO} with temperature.* The variation of I_{CBO} with temperature is less in silicon as compared to germanium. A rough rule of thumb for germanium is that I_{CBO} approximately doubles with each 8 to 10°C rise while in case of silicon, it approximately doubles with each 12°C rise.

(iii) *Greater working temperature.* The structure of germanium will be destroyed at a temperature of approximately 100°C. The maximum normal working temperature of germanium is 70°C but silicon can be operated upto 150°C. Therefore, silicon devices are not easily damaged by excess heat.

(iv) *Higher PIV rating.* The *PIV* ratings of silicon diodes are greater than those of germanium diodes. For example, the *PIV* ratings of silicon diodes are in the neighbourhood of 1000V whereas the *PIV* ratings of germanium diodes are close to 400V.

The disadvantage of silicon as compared to germanium is that potential barrier of silicon diode (0.7V) is more than that of germanium diode (0.5V). This means that higher bias voltage is required to cause current flow in a silicon diode circuit. This drawback of silicon goes to the background in view of the other advantages of silicon mentioned above. Consequently, the modern trend is to use silicon in semiconductor devices.

Example 9.36. *A small signal germanium transistor operating at 25°C has I_{CBO} = 5 μA, β = 40 and zero signal collector current = 2mA.*

(i) Find the collector cut- off current i.e. I_{CEO}.

(ii) Find the percentage change in zero signal collector current if the temperature rises to 55°C. Assume I_{CBO} doubles with every 10°C rise.

(iii) What will be the percentage change in silicon transistor under the same conditions? Given that I_{CBO} for silicon is 0.1μA at 25°C and I_{CBO} doubles for every 10°C rise.

Solution.

(i) $I_{CEO} = (\beta + 1)\, I_{CBO} = (40 + 1)\,(5\ \mu A) = 205\ \mu A = \mathbf{0.205\ mA}$

(ii) Rise in temperature = 55 – 25 = 30°C

Since I_{CBO} doubles for every 10°C rise, the new I_{CBO} in Ge transistor at 55°C will be 8 times that at 25°C *i.e.*

Now $I_{CBO} = 8 \times 5 = 40\ \mu A$

$\therefore$ $I_{CEO} = (\beta + 1)\, I_{CBO} = (40 + 1)\,(40\ \mu A) = 1640\ \mu A = 1.64\ mA$

$\therefore$ Zero signal collector current at 55°C

$= 2 + 1.64 = 3.64\ mA$

Percentage change in zero signal collector current

$$= \frac{3.64 - 2}{2} \times 100 = \mathbf{82\ \%}$$

i.e., zero signal collector current rises 82% above its original value due to 30°C rise in temperature.

(iii) With silicon transistor,

I_{CBO} = 0.1 μA at 25°C and β = 40

$\therefore$ $I_{CEO} = (\beta + 1)\, I_{CBO} = (40 + 1)\,(0.1\ \mu A)$

$= 4.1\ \mu A = 0.0041\ mA$

A 30°C rise in temperature would cause I_{CEO} in silicon to increase 8 times.

$$\text{Now } I_{CEO} = 8 \times 0.0041 = 0.0328\ mA$$

$\therefore$ Zero signal collector current at 55°C

$$= 2 + 0.0328 = 2.0328\ mA$$

Percentage change in zero signal collector current

$$= \frac{2.0328 - 2}{2} \times 100 = \mathbf{1.6\ \%}$$

i.e., increase in zero signal collector current is 1.6%.

Comments. The above example shows that change in zero signal collector current with rise in temperature is very small in silicon as compared to germanium. In other words, temperature effects very slightly change the operating point of silicon transistors while they may cause a drastic change in germanium transistors. This is one of the reasons that silicon has become the main semiconductor material in use today.

Example 9.37. *A silicon transistor has $I_{CBO} = 0.02\mu A$ at 27°C. The leakage current doubles for every 6°C rise in temperature. Calculate the base current at 57°C when the emitter current is 1mA. Given that $\alpha = 0.99$.*

Solution. A 30°C (57 – 27 = 30) rise in temperature would cause I_{CBO} to increase 32 times.

$\therefore$ At 57°C, $I_{CBO} = 32 \times 0.02 = 0.64\ \mu A = 0.00064\ mA$

$$\text{Now } I_C = \alpha I_E + I_{CBO}$$

$$= 0.99 \times 1 + 0.00064 = 0.9906\ mA = 0.000\ 64\ mA$$

$\therefore$ $I_B = I_E - I_C = 1 - 0.9906 = 0.0094\ mA = \mathbf{9.4\ \mu A}$

9.19 Instantaneous Current and Voltage Waveforms

It is worthwhile to show instantaneous current and voltage waveforms in an amplifier. Consider a *CE* amplifier biased by base resistor method as shown in Fig. 9.44. Typical circuit values have been assumed to make the treatment more illustrative. Neglecting V_{BE}, it is clear that zero signal base current $I_B = V_{CC}/R_B = 20\ V/1M\Omega = 20\ \mu A$. The zero signal collector current $I_C = \beta I_B = 100 \times 20\ \mu A = 2mA$. When signal of peak current 10 μA is applied, alternating current is superimposed on the d.c. base current. The collector current and collector-emitter voltage also vary as the signal changes. The instantaneous waveforms of currents and voltages are shown in Fig. 9.45. Note that base current, collector current and collector-emitter voltage waveforms are composed of (*i*) the d.c. component and (*ii*) the a.c. wave riding on the d.c.

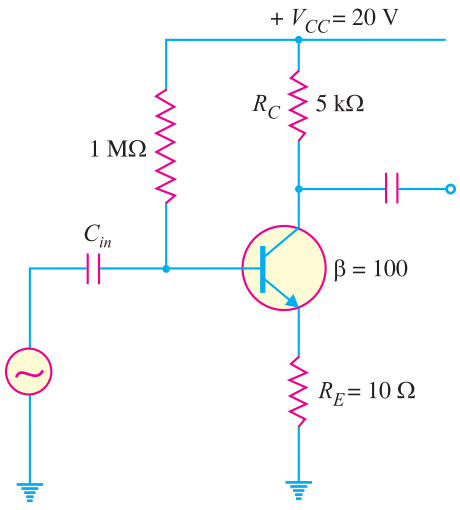


Fig. 9.44

(*i*) At π/2 radians, the base current is composed of 20 μA d.c. component plus 10 μA peak a.c. component, adding to 30 μA *i.e* $i_B = 20 + 10 = 30\ \mu A$. The corresponding collector current $i_C = 100 \times 30\ \mu A = 3$ mA. The corresponding collector-emitter voltage is

$$v_{CE} = V_{CC} - i_C R_C = 20\ V - 3\ mA \times 5\ k\Omega$$

$$= 20\ V - 15\ V = 5\ V$$

Note that as the input signal goes positive, the

collector current increases and collector-emitter voltage decreases. Moreover, during the positive half cycle of the signal (*i.e.* from 0 to π rad.), the operating point moves from 20 μA to 20 + 10 = 30 μA and then back again *i.e.* operating point follows the path *Q* to *C* and back to *Q* on the load line.

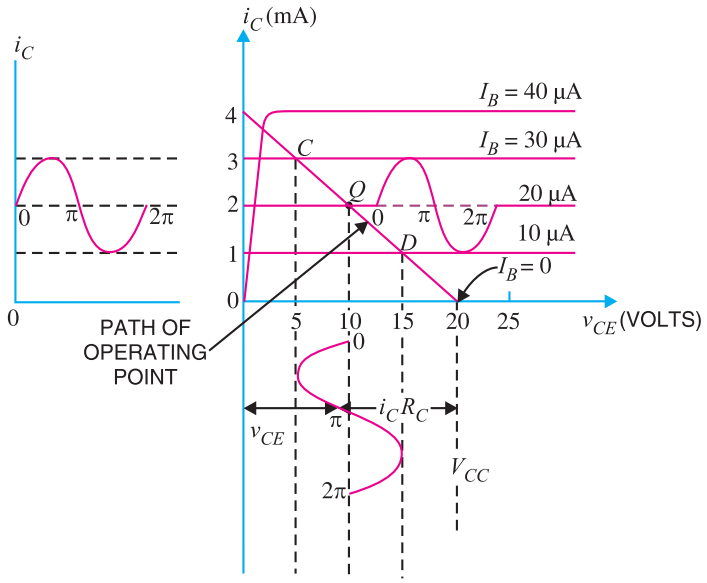


Fig. 9.45

(ii) During the negative half-cycle of the signal (from π to 2π rad.), the operating point goes from 20 μA to 20 – 10 = 10 μA and then back again *i.e.* the operating point follows the path *Q* to *D* and back to *Q* on the load line.

(iii) As the operating point moves along the path *CD* or *DC* due to the signal, the base current varies continuously. These variations in the base current cause both collector current and collector-emitter voltage to vary.

(iv) Note that when the input signal is maximum positive, the collector-emitter voltage is maximum negative. In other words, input signal voltage and output voltage have a phase difference of 180°. This is an important characteristic of *CE* arrangement.

Example 9.38. *What fault is indicated in Fig. 9.46 ? Explain your answer with reasons.*

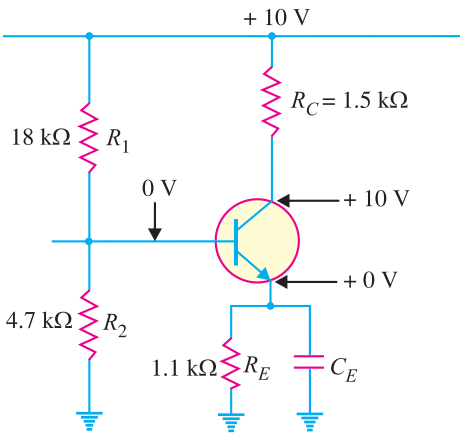


Fig. 9.46

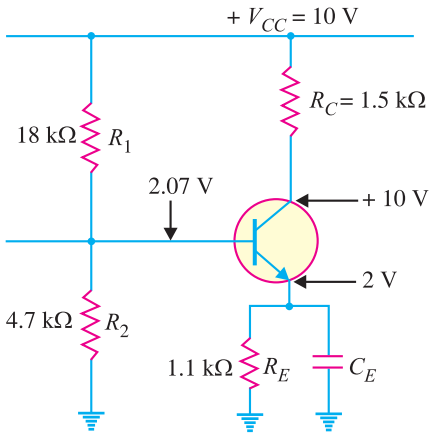


Fig. 9.47

Solution. Since V_B (*i.e.*, base voltage *w.r.t.* ground) is zero, it means that there is no path for current in the base circuit. The transistor will be biased off *i.e.*, $I_C = 0$ and $I_E = 0$. Therefore, $V_C = 10$ V ($\because I_C R_C = 0$) and $V_E = 0$. The obvious fault is that R_1 is open.

Example 9.39. *What fault is indicated in Fig. 9.47? Explain your answer with reasons.*

Solution. Based on the values of R_1, R_2 and V_{CC}, the voltage V_B at the base seems appropriate. In fact it is so as shown below :

$$\text{Voltage at base, } V_B = \text{Voltage across } R_2$$

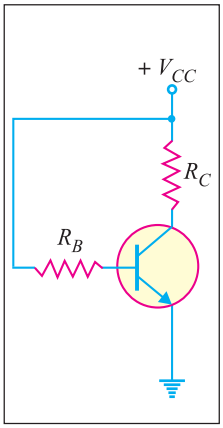
$$= \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{10}{18 + 4.7} \times 4.7 = 2.07 \text{ V}$$

The fact that $V_C = +10$ V and $V_E \simeq V_B$ reveals that $I_C = 0$ and $I_E = 0$. As a result, I_B drops to zero. The obvious fault is that R_E is open.

9.20 Summary Of Transistor Bias Circuits

In figures below, *npn* transistors are shown. Supply voltage polarities are reversed for *pnp* transistors.

BASE BIAS

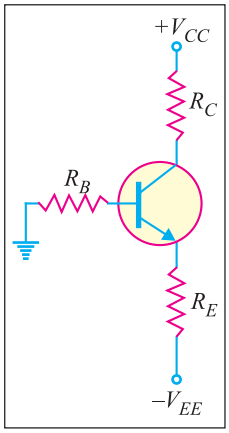


- Q-point values ($I_C \simeq I_E$)
- Collector current:

$$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$$

- Collector-to-emitter voltage:
- $V_{CE} = V_{CC} - I_C R_C$

EMITTER BIAS

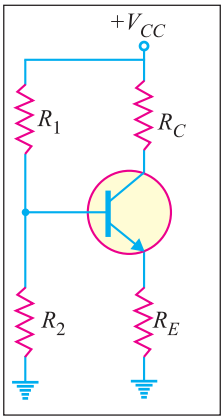


- Q-point values ($I_C \simeq I_E$)
- Collector current:

$$I_C \simeq \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

- Collector-to-emitter voltage:
- $V_{CE} \simeq V_{CC} - V_{CE} - I_C(R_C + R_E)$

VOLTAGE-DIVIDER BIAS

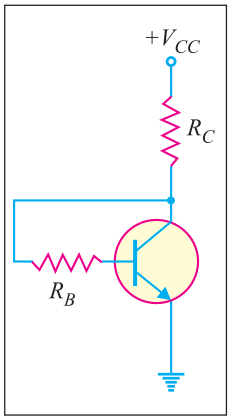


- Q-point values ($I_C \simeq I_E$)
- Collector current:

$$I_C \simeq \frac{\left(\frac{R_2}{R_1 + R_2}\right)V_{CC} - V_{BE}}{R_E}$$

- Collector-to-emitter voltage:
- $V_{CE} \simeq V_{CC} - I_C(R_C + R_E)$

COLLECTOR-FEEDBACK BIAS



- Q-point values ($I_C \simeq I_E$)
- Collector current:

$$I_C \simeq \frac{V_{CC} - V_{BE}}{R_C + R_B/\beta}$$

- Collector-to-emitter voltage:
- $V_{CE} = V_{CC} - I_C R_C$

MULTIPLE-CHOICE QUESTIONS

1. Transistor biasing represents ..... conditions.
(*i*) a.c.
(*ii*) d.c.
(*iii*) both a.c. and d.c.
(*iv*) none of the above

2. Transistor biasing is done to keep ..... in the circuit.
(*i*) proper direct current
(*ii*) proper alternating current
(*iii*) the base current small
(*iv*) collector current small

3. Operating point represents ..... .
(*i*) values of I_C and V_{CE} when signal is applied
(*ii*) the magnitude of signal
(*iii*) zero signal values of I_C and V_{CE}
(*iv*) none of the above

4. If biasing is not done in an amplifier circuit, it results in .....
(*i*) decrease in base current
(*ii*) unfaithful amplification
(*iii*) excessive collector bias
(*iv*) none of the above

5. Transistor biasing is generally provided by a .....
(*i*) biasing circuit (*ii*) bias battery
(*iii*) diode (*iv*) none of the above

6. For faithful amplification by a transistor circuit, the value of V_{BE} should ..... for a silicon transistor.
(*i*) be zero
(*ii*) be 0.01 V
(*iii*) not fall below 0.7 V
(*iv*) be between 0 V and 0.1 V

7. For proper operation of the transistor, its collector should have .....
(*i*) proper forward bias
(*ii*) proper reverse bias
(*iii*) very small size
(*iv*) none of the above

8. For faithful amplification by a transistor circuit, the value of V_{CE} should ..... for silicon transistor.
(*i*) not fall below 1 V
(*ii*) be zero
(*iii*) be 0.2 V
(*iv*) none of the above

9. The circuit that provides the best stabilisation of operating point is .....
(*i*) base resistor bias
(*ii*) collector feedback bias
(*iii*) potential divider bias
(*iv*) none of the above

10. The point of intersection of d.c. and a.c. load lines represents .....
(*i*) operating point (*ii*) current gain
(*iii*) voltage gain (*iv*) none of the above

11. An ideal value of stability factor is .....
(*i*) 100 (*ii*) 200
(*iii*) more than 200 (*iv*) 1

12. The zero signal I_C is generally ..... mA in the initial stages of a transistor amplifier.
(*i*) 4 (*ii*) 1
(*iii*) 3 (*iv*) more than 10

13. If the maximum collector current due to signal alone is 3 mA, then zero signal collector current should be atleast equal to .....
(*i*) 6 mA (*ii*) 1.5 mA
(*iii*) 3 mA (*iv*) 1 mA

14. The disadvantage of base resistor method of transistor biasing is that it .....
(*i*) is complicated
(*ii*) is sensitive to changes in β
(*iii*) provides high stability
(*iv*) none of the above

15. The biasing circuit has a stability factor of 50. If due to temperature change, I_{CBO} changes by 1 μA, then I_C will change by .....
(*i*) 100 μA (*ii*) 25 μA
(*iii*) 20 μA (*iv*) 50 μA

16. For good stabilisation in voltage divider bias,

the current I_1 flowing through R_1 and R_2 should be equal to or greater than .....

(*i*) 10 I_B (*ii*) 3 I_B

(*iii*) 2 I_B (*iv*) 4 I_B

17. The leakage current in a silicon transistor is about ..... the leakage current in a germanium transistor.

(*i*) one hundredth (*ii*) one tenth

(*iii*) one thousandth (*iv*) one millionth

18. The operating point is also called the .....

(*i*) cut off point

(*ii*) quiescent point

(*iii*) saturation point

(*iv*) none of the above

19. For proper amplification by a transistor circuit, the operating point should be located at ..... of the d.c. load line.

(*i*) the end point

(*ii*) middle

(*iii*) the maximum current point

(*iv*) none of the above

20. The operating point ..... on the a.c. load line.

(*i*) also lies (*ii*) does not lie

(*iii*) may or may not lie

(*iv*) data insufficient

21. The disadvantage of voltage divider bias is that it has .....

(*i*) high stability factor

(*ii*) low base current

(*iii*) many resistors

(*iv*) none of the above

22. Thermal runaway occurs when .....

(*i*) collector is reverse biased

(*ii*) transistor is not biased

(*iii*) emitter is forward biased

(*iv*) junction capacitance is high

23. The purpose of resistance in the emitter circuit of a transistor amplifier is to .....

(*i*) limit the maximum emitter current

(*ii*) provide base-emitter bias

(*iii*) limit the change in emitter current

(*iv*) none of the above

24. In a transistor amplifier circuit, $V_{CE} = V_{CB} +$ .....

(*i*) V_{BE} (*ii*) 2 V_{BE}

(*iii*) 1.5 V_{BE} (*iv*) none of the above

25. The base resistor method is generally used in .....

(*i*) amplifier circuits

(*ii*) switching circuits

(*iii*) rectifier circuits

(*iv*) none of the above

26. For germanium transistor amplifier, V_{CE} should ..... for faithful amplification.

(*i*) be zero

(*ii*) be 0.2 V

(*iii*) not fall below 0.7 V

(*iv*) none of the above

27. In a base resistor method, if the value of β changes by 50, then collector current will change by a factor of .....

(*i*) 25 (*ii*) 50

(*iii*) 100 (*iv*) 200

28. The stability factor of a collector feedback bias circuit is ..... that of base resistor bias.

(*i*) the same as (*ii*) more than

(*iii*) less than (*iv*) none of the above

29. In the design of a biasing circuit, the value of collector load R_C is determined by .....

(*i*) V_{CE} consideration

(*ii*) V_{BE} consideration

(*iii*) I_B consideration

(*iv*) none of the above

30. If the value of collector current I_C increases, then value of V_{CE} .....

(*i*) remains the same

(*ii*) decreases

(*iii*) increases

(*iv*) none of the above

31. If the temperature increases, the value of V_{BE} .....

(*i*) remains the same

(*ii*) is increased

(*iii*) is decreased

(*iv*) none of the above

32. The stabilisation of operating point in potential divider method is provided by .....
(*i*) R_E consideration
(*ii*) R_C consideration
(*iii*) V_{CC} consideration
(*iv*) none of the above

33. The value of V_{BE} .....
(*i*) depends upon I_C to moderate extent
(*ii*) is almost independent of I_C
(*iii*) is strongly dependent on I_C
(*iv*) none of the above

34. When the temperature changes, the operating point is shifted due to .....
(*i*) change in I_{CBO}
(*ii*) change in V_{CC}
(*iii*) change in the values of circuit resistances
(*iv*) none of the above

35. The value of stability factor for a base-resistor bias is .....
(*i*) $R_B(\beta + 1)$ (*ii*) $(\beta + 1) R_C$
(*iii*) $(\beta + 1)$ (*iv*) $1 - \beta$

36. In a practical biasing circuit, the value of R_E is about .....
(*i*) 10 kΩ (*ii*) 1 MΩ
(*iii*) 100 kΩ (*iv*) 800 Ω

37. A silicon transistor is biased with base resistor method. If $\beta = 100$, $V_{BE} = 0.7$ V, zero signal collector current $I_C = 1$ mA and $V_{CC} = 6$ V, what is the value of base resistor R_B ?
(*i*) 105 kΩ (*ii*) 530 kΩ
(*iii*) 315 kΩ (*iv*) none of the above

38. In voltage divider bias, $V_{CC} = 25$ V ; $R_1 = 10$ kΩ; $R_2 = 2.2$ kΩ ; $R_C = 3.6$ kΩ and $R_E = 1$ kΩ. What is the emitter voltage ?
(*i*) 6.7 V (*ii*) 5.3 V
(*iii*) 4.9 V (*iv*) 3.8 V

39. In the above question, what is the collector voltage ?
(*i*) 12.3 V (*ii*) 14.8 V
(*iii*) 7.6 V (*iv*) 9.7 V

40. In voltage divider bias, operating point is 3 V, 2 mA. If $V_{CC} = 9$ V, $R_C = 2.2$ kΩ, what is the value of R_E ?
(*i*) 2000 Ω (*ii*) 1400 Ω
(*iii*) 800 Ω (*iv*) 1600 Ω

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*i*)	**3.** (*iii*)	**4.** (*ii*)	**5.** (*i*)
6. (*iii*)	**7.** (*ii*)	**8.** (*i*)	**9.** (*iii*)	**10.** (*i*)
11. (*iv*)	**12.** (*ii*)	**13.** (*iii*)	**14.** (*ii*)	**15.** (*iv*)
16. (*i*)	**17.** (*iii*)	**18.** (*ii*)	**19.** (*ii*)	**20.** (*i*)
21. (*iii*)	**22.** (*ii*)	**23.** (*iii*)	**24.** (*i*)	**25.** (*ii*)
26. (*iii*)	**27.** (*ii*)	**28.** (*iii*)	**29.** (*i*)	**30.** (*ii*)
31. (*iii*)	**32.** (*i*)	**33.** (*ii*)	**34.** (*i*)	**35.** (*iii*)
36. (*iv*)	**37.** (*ii*)	**38.** (*iv*)	**39.** (*i*)	**40.** (*iii*)

Chapter Review Topics

1. What is faithful amplification ? Explain the conditions to be fulfilled to achieve faithful amplification in a transistor amplifier.

2. What do you understand by transistor biasing ? What is its need ?

3. What do you understand by stabilisation of operating point ?

4. Mention the essentials of a biasing circuit.

5. Describe the various methods used for transistor biasing. State their advantages and disadvantages.

6. Describe the potential divider method in detail. How stabilisation of operating point is achieved by this method ?

7. Mention the steps that are taken to design the transistor biasing and stabilisation circuits.

8. Write short notes on the following :

(*i*) Operating point (*ii*) Stabilisation of operating point

Problems

1. An *npn* silicon transistor has V_{CC} = 5V and the collector load R_C = 2 kΩ. Find :

(*i*) the maximum collector current that can be allowed during the application of signal for faithful amplification

(*ii*) the minimum zero signal collector current required **[(*i*) 2mA (*ii*) 1mA]**

2. Fig. 9.48 shows biasing with base resistor method. Determine the operating point. Assume the transistor to be of silicon and take β = 100. **[I_C = 0.93 mA, V_{CE} = 17.3V]**

3. Fig. 9.49 shows biasing by base resistor method. If it is required to set the operating point at 1mA, 6 V, find the values of R_C and R_B. Given β =150, V_{BE} = 0.3 V. **[R_C = 3 kΩ, R_B = 0.3 MΩ]**

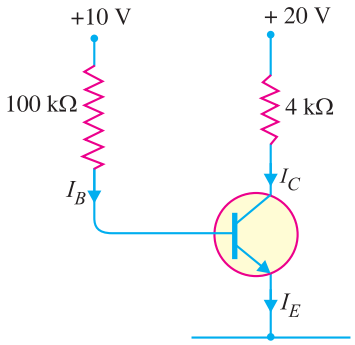


Fig. 9.48

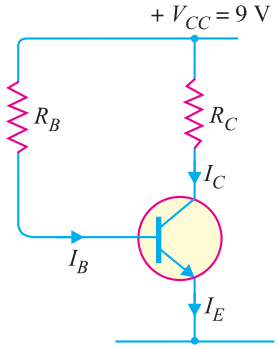


Fig. 9.49

4. A transistor amplifier is biased with feedback resistor R_B of 100 kΩ. If V_{CC} = 25 V, R_C = 1 kΩ and β = 200, find the values of zero signal I_C and V_{CE}. **[I_C = 16.2mA, V_{CE} = 8.8V]**

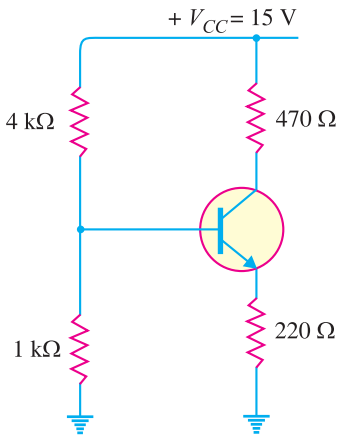


Fig. 9.50

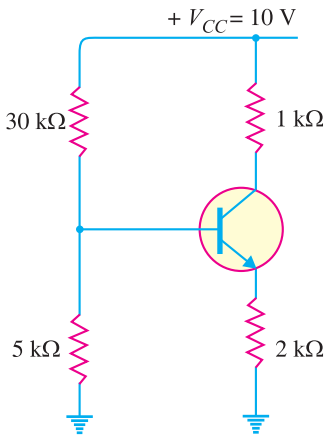


Fig. 9.51

5. Find the value of I_C for potential divider method if V_{CC} = 9V, R_E = 1kΩ, R_1 = 39 kΩ, R_2 = 10 kΩ, R_C = 2.7 kΩ, V_{BE} = 0.15 V and β = 90. **[1.5mA]**

6. In an *RC* coupled amplifier, the battery voltage is 16V and collector load R_C = 4 kΩ. It is required to set the operating point at I_C = 1mA, V_{CE} = 10V by potential divider method. If V_{BE} = 0.2 V and $I_1 = 10\ I_B$, β = 100, find the various circuit values.

7. In the transistor circuit shown in Fig. 9.50, find the operating point. Assume the transistor to be of silicon. **[I_C = 10.5mA, V_{CE} = 7.75V]**

8. In a transistor circuit shown in Fig. 9.51, find the operating point. Assume silicon transistor is used. **[I_C = 0.365mA, V_{CE} = 8.9V]**

9. Determine whether or not the circuit shown in Fig. 9.52 is midpoint biased. **[Yes]**

10. What fault is indicated in Fig. 9.53 ? Give reasons for your answer. **[R_C is open]**

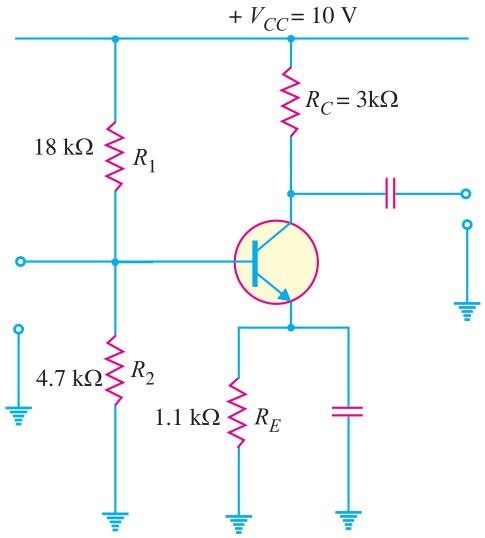


Fig. 9.52

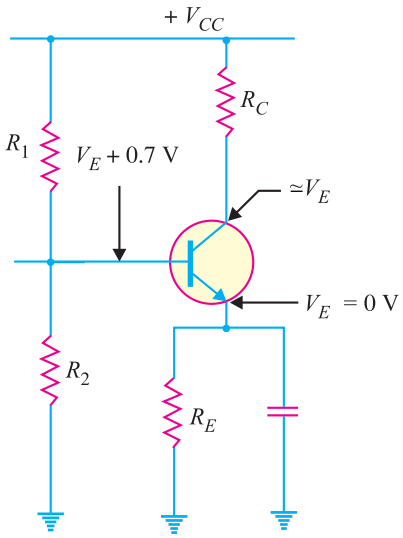


Fig. 9.53

11. Determine I_B, I_C and V_{CE} for a base-biased transistor circuit with the following values : β = 90 ; V_{CC} = 12V; R_B = 22 kΩ and R_C = 100Ω. **[I_B = 514 μA ; I_C = 46.3 mA ; V_{CE} = 7.37V]**

12. The base bias circuit in Fig. 9.54 is subjected to a temperature variation from 0°C to 70°C. The β decreases by 50% at 0°C and increases by 75% at 70°C from its normal value of 110 at 25°C. What are the changes in I_C and V_{CE} over the temperature range of 0°C to 70°C ?

[I_C = 59.6 mA ; V_{CE} = 5.96V]

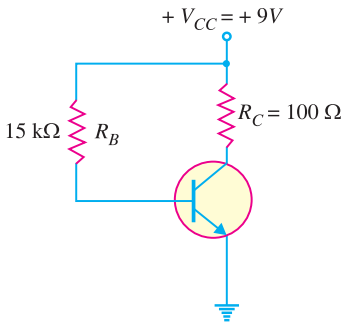


Fig. 9.54

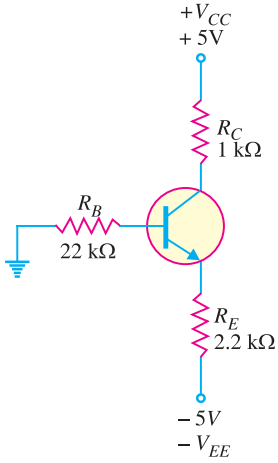


Fig. 9.55

13. To what value can R_E in Fig. 9.55 be reduced without transistor going into saturation ? **[639Ω]**

14. When can the effect of β be neglected in the emitter bias circuit ? **[When $R_E >> R_B/\beta$]**

15. What is the minimum value of β in Fig. 9.56 that makes $R_{in\ (base)} \geq 10\ R_2$? **[69.1]**

16. (*i*) Determine the base voltage V_B in Fig. 9.57.
(*ii*) If R_E is doubled, what will be the value of V_B ? **[(*i*) 1.74V (*ii*) 1.74V]**

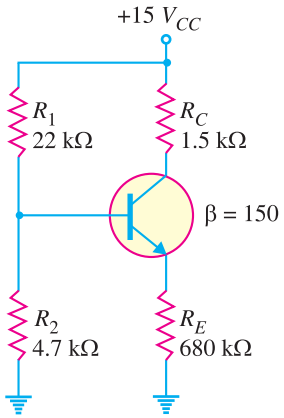


Fig.9.56

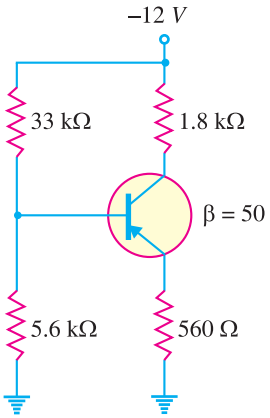


Fig. 9.57

17. (*i*) Find the Q-point values for Fig. 9.57.
(*ii*) Find the minimum power rating of transistor in Fig. 9.57. **[(*i*) 1.41 mA ; – 8.67V (*ii*) 12.2 mW]**

18. A collector-feedback circuit uses an *npn* transistor with V_{CC} = 12V, R_C = 1.2 kΩ, R_B = 47 kΩ. Determine the collector voltage and the collector current if β = 200. **[7.87 mA ; 2.56V]**

Discussion Questions

1. Why are transistor amplifiers always operated above knee voltage region ?

2. What is the utility of d.c. load line ?

3. Why have transistors inherent variations of parameters ?

4. Why is $\beta_{d.c.}$ different from $\beta_{a.c.}$?

5. Why has potential divider method of biasing become universal ?

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